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Power Electronic Converter Reliability Improvement Optimization Using Genetic Algorithm

Felix Adabla

POWER ELECTRONIC CONVERTER RELIABILITY IMPROVEMENT OPTIMIZATION USING GENETIC ALGORITHM

by

FELIX ADABLA

(Under the Direction of Masoud Davari)

ABSTRACT

Power electronic converter (PEC) systems are vital for efficient and reliable electrical energy conversion across various applications. Since the overall reliability of these applications is determined, to some degree, by the reliability of the PECs that form the foundation of these applications, it is essential to explore the reliability improvement strategies adopted for these PECs. In fact, various works have been done in that regard. However, another question that arises from these reliability improvement strategies is "how much is enough" since improvement in one area might be at the cost of another factor. In an attempt to answer this question, this thesis addresses the growing demand for improved converter systems' reliability by proposing a reliability improvement optimization approach using Genetic Algorithm. The research investigates established reliability models for critical converter components and formulates various single and multi-objective optimization problems based on the models. Key parameters influencing failure rate and Mean Time To Failure were identified and integrated into the Genetic Algorithm framework. The framework combined Genetic Algorithm with the selected reliability prediction models, enabling a systematic exploration of the design space. Factors like component sizing, thermal management, switching frequency, and redundancy strategy are considered during the problem formulation.

INDEX WORDS: Active thermal control, Bathtub curve, Capacitor lifetime, Design for reliability, Genetic Algorithm, MTTF, Multi-objective optimization, Single-objective optimization, Switching device cycles to failure, Thermal stress

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DEDICATION

First and foremost, to my dearest parents, Mr. Patrick Adabla and Mrs. Selina Adabla, this work is a testament to the spark you first ignited within me. Your unwavering support throughout my education instilled a love of learning that fueled this journey. This thesis would not be possible without your constant belief in my potential and the sacrifices you made to put me through school. Thank you for empowering me to reach for the stars.

Secondly, to all the inspiring teachers and professors who have guided me since my days in William De-Graft, Pere Planque, Mfantsipim, and KNUST, this thesis is a tribute to your dedication. Each of you played a vital role in shaping my academic foundation and career path and nurturing my curiosity. Thank you for fostering my intellectual growth and believing in a student who might not have always believed in himself.

Thirdly, this thesis is dedicated to the person I was at the beginning of this journey, filled with questions and a thirst for knowledge. Thank you for embarking on this exploration and for the incredible person you have become. May this thesis stand as a tribute to the collective effort and belief in the power of knowledge and education to shape our lives and the world.

Finally, as Ralph Waldo Emerson so eloquently stated, “What lies behind us and what lies before us are tiny matters compared to what lies within us.” This thesis is dedicated to the engineers striving for ever-more reliable power electronic converters. Your dedication highlights the importance of reliability in power converters, which are critical systems in the electrical engineering field.

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$\Delta T_{Cap,cycling}$ . . . . . Capacitor core temperature rise

$\Delta T_{SD,J}$ . . . . . SD junction temperature swing

ΔT_{bw} . . . . . SD bond wire temperature difference

λ_{0Cap} . . . . . Basic failure rate of a capacitor

λ_{0Mech} . . . . . Mechanical stress basic failure rate of the SD

λ_{0RH} . . . . . Relative humidity basic failure rate of the SD

$\lambda_{0TCyCase}$ . . . . . Thermal cycling basic failure rate of the SD

$\lambda_{0TCySolderJoints}$ . . . . . Solder joints thermal cycling basic failure rate

λ_{0TH} . . . . . Thermal contribution basic failure rate of the SD

$\lambda_{Cap,useful}$ . . . . . Useful failure rate of a capacitor

$\lambda_{Cap,wear}$ . . . . . Wear-out failure rate of a capacitor

$\lambda_{PEC,useful}$ . . . . . Useful failure rate of converter, $[FIT]$

$\lambda_{PEC,wear}$ . . . . . Wear-out failure rate of converter, $[FIT]$

λ_{PEC} . . . . . Failure rate of power electronic converter system

$\lambda_{S,Cap}$ . . . . . Capacitor system failure rate (redundancy)

$\lambda_{SD,useful}$ . . . . . Useful failure rate of a SD

$\lambda_{SD,wear}$ . . . . . Wear-out failure rate of a SD

ρ_{bw} . . . . . Bond wire resistivity, $[\Omega m]$

σ . . . . . Stefan-Boltzmann's constant

ε . . . . . Radiation thermal coefficient/emissivity

A_{Cap} . . . . . Surface area of the electrolytic capacitor, $[m^2]$

A_{hs} . . . . . Surface area of the heat sink

C . . . . . Capacitance, $[F]$

$Cost_{Comp}$ . . . . . Cost of the component, [$]

D_{Cap} . . . . . Diameter of the electrolytic capacitor, $[m]$

D_{ox} . . . . . Dissipation factor of the dielectric layer

$D_{SD,bw}$ . . . . . Diameter of the SD bond wire, $[m]$

$DuCy$ . . . . . Duty cycle of the application

$E_{Cap,a}$ . . . . . Activation energy of the capacitor

$E_{SD,a}$ . . . . . Activation energy of switching device, $[0.9eV]$

$E_{sw,ref}$ . . . . . Reference switching energy loss of SD, $[J]$

E_{sw} . . . . . Switching energy loss ($E_{on} + E_{off}$), $[J]$

f_{sw} . . . . . Switching frequency of the application, $[Hz]$

G_{RMS_0} . . . . . Reference vibration amplitude

G_{RMS} . . . . . RMS value of the vibration amplitude

h_{free} . . . . . Capacitor convection heat transfer coefficient

h_{rad} . . . . . Capacitor radiation heat transfer coefficient

h_{tot} . . . . . Capacitor total heat transfer coefficient, $[W/mK]$

I_{rip} . . . . . Percent ripple current of the rated current

$i_{SD,c}$ . . . . . Collector current of the switching device

K_B . . . . . Boltmann's constant (in eV/K)

k_{bw} . . . . . Bond wire thermal conductivity, $[W/mK]$

$K_{Cap,i}$ . . . . . Empirical safety factor of the capacitor

k_{hs} . . . . . Thermal conductivity of the heatsink, $[W/mK]$

L_0 . . . . . Nominal lifetime of the capacitor, $[yrs]$

l_{bw} . . . . . Length of the SD bond wire, $[m]$

L_{Cap} . . . . . Length of the capacitor

N_{Cap} . . . . . Number of capacitors

$N_{f,SD}$ . . . . . Switching device's cycles to failure

N_{SD} . . . . . Number of switching devices

P_A . . . . . Average total power loss in a SD, $[W]$

$P_{SD,Cond}$ . . . . . Conduction loss of switching device, $[W]$

$P_{SD,Sw}$ . . . . . Switching device switching loss, $[W]$

R^2 . . . . . Coefficient of determination

R_d . . . . . Dielectric frequency-dependent resistance, $[\Omega]$

R_e . . . . . Capacitor temperature-dependent resistance, $[\Omega]$

R_o . . . . . Constant ohmic resistance of the capacitor, $[\Omega]$

$R_{Cap,th}$ . . . . . Thermal resistance of the capacitor, $[°C/W]$

$R_{hs,th}$ . . . . . Thermal resistance of the heat sink

$R_{SD,On}$ . . . . . SD on-state resistance

$R_{SD,th}$ . . . . . Thermal resistance of the SD, $[°C/W]$

RH_0 . . . . . Reference relative humidity

RH_{amb} . . . . . Ambient relative humidity

$Space_{pcb}$ . . . . . Allocated component area/space on the PCB, $[m^2]$

T_{amb} . . . . . Ambient temperature, $[°C]$

T_{annual} . . . . . Total hours in one year

$T_{Cap,c}$ . . . . . Core temperature of the capacitor, $[°C]$

$T_{Cap,max-cycling}$ . . . . . Maximum temperature of the capacitor, $[°C]$

$t_{hs,b}$ . . . . . Switching device's heat sink base thickness, $[m]$

t_{on} . . . . . Power-on-time, $[s]$

t_{phase} . . . . . During of the operation phase, $[hrs]$

$T_{SD,J,max}$ . . . . . Maximum junction temperature of the SD, $[°C]$

$T_{SD,J}$ . . . . . Mean junction temperature value, $[°C]$

TC_{sw} . . . . . Temperature coefficient of switching energy loss

$V_{applied}$ . . . . . Application voltage of operation

v_{ce0} . . . . . On-state zero-current collector-emitter voltage

V_{rated} . . . . . Rated voltage of the component

$v_{SD,ce}$ . . . . . Off-state collector-emitter voltage

LIST OF ACRONYMS

AC . . . . . Alternating current

AF . . . . . Acceleration factor

ANN . . . . . Artificial neural network

AR . . . . . Aspect ratio

ATC . . . . . Active thermal control

Cap . . . . . Capacitor

CTE . . . . . Coefficient of thermal expansion

Cu . . . . . Copper

DC . . . . . Direct current

EOS . . . . . Electrical Overstress

ESR . . . . . Equivalent series resistance

EV . . . . . Electric vehicle

FIDES . . . . . Fiabilité des Equipements Développés en Série

FIT . . . . . Failures in time

FR . . . . . Failure rate

FTC . . . . . Fault-tolerant control

GA . . . . . Genetic Algorithm

GaN . . . . . Gallium Nitride

HVAC . . . . . High-voltage ac

HVDC . . . . . High-voltage dc

IGBT . . . . . Insulated Gate Bipolar Transister

MILP . . . . . Mixed integer linear programming

MMC . . . . . Modular multilevel converter

MOOP . . . . . Multi-objective optimization problem

MOS . . . . . Mechanical overstress

MOSFET . . . . . Metal-Oxide-Silicon-Field-Effect-Transister

MTTF . . . . . Mean time to failure

NPC . . . . . Neutral point clamped

PCB . . . . . Printed circuit board

PEC . . . . . Power electronic converter

PHM . . . . . Prognostic and health management

PoF . . . . . Physics-of-Failure

PV . . . . . Photovoltaic

PWM . . . . . Pulse width modulation

QA . . . . . Quality Assurance

RA . . . . . Reliability Assurance

RMS . . . . . Root mean square

SD . . . . . Semiconductor/Switching device

Si . . . . . Silicon

SiC . . . . . Silicon Carbide

SMD . . . . . Surface mounted device

SOOP . . . . . Single-objective optimization problem

TOS . . . . . Thermal overstress

WT . . . . . Wind turbine

CHAPTER 1

INTRODUCTION

In the contemporary landscape of energy conversion and electronic systems, power electronic converter (PEC) systems play a pivotal role in facilitating the efficient and controlled flow of electrical energy. PEC systems are contemporary fundamental systems employed in various applications and industries including but not limited to transportation (hybrid and fully-electric cars[1], aircraft power supplies, locomotives, and elevators); power generation, storage and distribution (renewables, nuclear field, hydro, gas turbines, HVDC); home appliances (blenders, audio speakers, computers, air-conditioners) and heavy industrial applications (motor drives, conveyors, cement kiln) [4],[13]. The automotive industry, for instance, has seen a recent boom thanks to new advances in PECs and semiconductors. Figure 1.1 and 1.2 and below is an excerpt of a typical DC-DC converter application in a hybrid/electric vehicle. These PECs can change voltage, frequency, current and even phase at will, letting engineers design efficient electrical systems for engines, batteries, and other parts. This efficiency is a key benefit of PEC systems because it essentially translates to the usage of less material, simpler cooling mechanisms, and higher energy efficiencies - saving money and using less material.

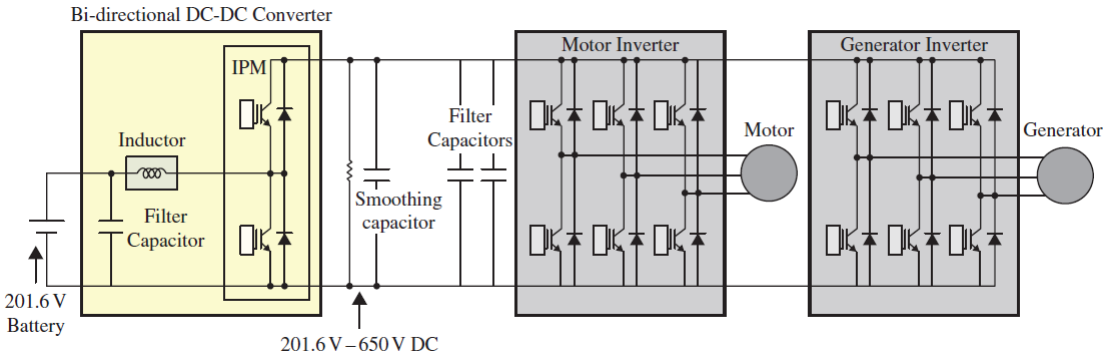


Figure 1.1: A 2010 Toyota Prius power controller [31].

Figure 1.3 on the other hand also shows a PEC's relevance in renewable energy generation, specifically in a wind turbine (WT) application. In the case of the EV, PECs regulate the charging and discharging of the vehicle's battery pack by ensuring that the vehicle receives the appropriate voltage and current levels during charging and that energy is efficiently delivered to the vehicle's electrical systems during discharging. Besides converting DC power from the battery into AC power

[1]This PEC application is in reference to Figure 1.1.

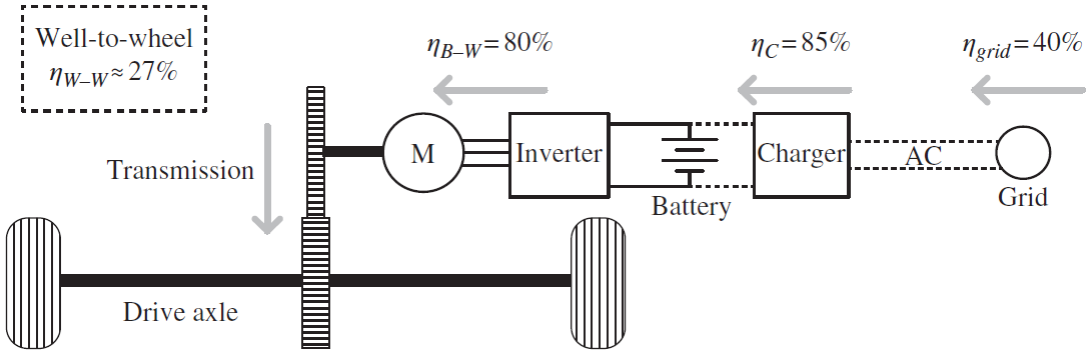


Figure 1.2: How PECs manage power flow in battery electric vehicles [31].

to drive the electric motor, the motor inverter PECs also control the speed and torque of the motors by adjusting the frequency and amplitude of the electrical signals supplied to them, which in turn allows for precise control of the vehicle's acceleration, deceleration, and overall performance. Furthermore, EVs typically operate on a high-voltage battery system, while many auxiliary systems (such as lights, HVAC, and infotainment) operate on lower voltages. PECs perform DC/DC conversion to step down the high-voltage battery power to the appropriate levels for these auxiliary systems, ensuring efficient power distribution throughout the vehicle.

Table 1.1: Application-specific lifetime goals for power converters [22], [23].

Applications	**Typical design target of lifetime**
Aircraft	24 years (100,000 hours flight operation)
Automotive	15 years (10,000 operating hours, 300,000 km)
Industry motor drives	5-20 years (60,000 hours at full load)
Railway	20-30 years (73,000-110,000 hours)
Wind turbines	20 years (120,000 hours)
Photovoltaic plants	30 years (90,000 - 130,000 hours)

Considering the above discussions on some of the modern applications of PECs, it is apparent why the growing demand for efficient power conversion in industrial applications has propelled the significance of PEC systems. Due to the crucial role that PEC systems play in converting and controlling electrical energy, they influence the overall performance and reliability of diverse power-based technologies. In other words, PEC systems have a direct/indirect influence on the estimated

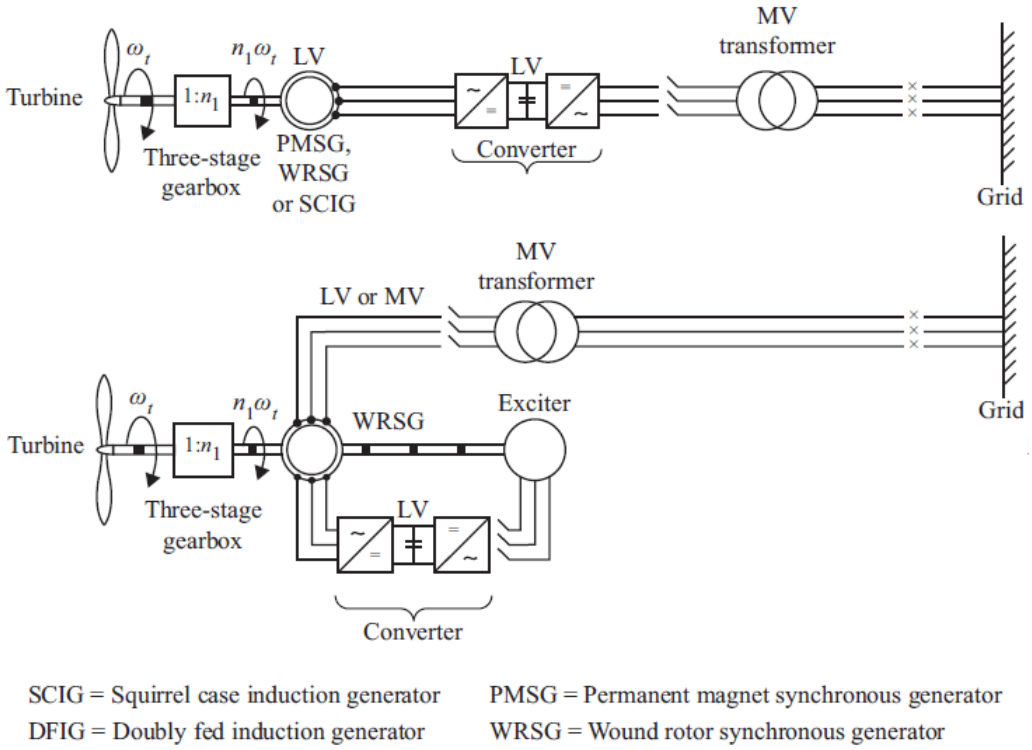


Figure 1.3: Utilization of PECs in the conversion of wind turbine energy [22].

lifetime of various industrial systems. To drive this point home, Table 1.1 is referenced to show the estimates of the typical design lifetime of some of the major industries that heavily depend on PECs. This discussion is to establish the fact that poor reliability on the part of PEC would directly translate to a decreased estimated lifetime of the highlighted application. Therefore, to maintain the desired lifetime of the application it is important to evaluate the reliability from the PEC level and even further from the component level [60].

A critical observation has shown that ensuring the robustness and reliability of power systems remains a complex and critical challenge, particularly in the face of varying operating conditions, environmental factors, and load dynamics [14]. Understandably, as the demand for reliable and high-performance electronic systems intensifies, we see an equivalent increase in the pertaining research as well as the implementation done to improve the reliability of PEC systems [23], [29], [36], [68].

Purpose of the Study

As seen from the above discussions, the reliability of power electronic converters is a key

aspect that directly influences the performance, longevity, and reliability of high-level power systems. It is worth mentioning, though, that their inherent complexities, coupled with the diverse and challenging operating conditions they often encounter in their applications, necessitate innovative approaches to enhance their reliability. In any given application, taking the aviation industry, for instance, PECs, including inverters, rectifiers, and DC-DC converters, are subjected to dynamic and diverse operational conditions. Factors such as mechanical vibrations may eventually lead to component dislodge or lift-off; current and voltage transients may also contribute to an increase in mean junction temperature ($T_{SD,J}$) and junction temperature variations ($\Delta T_{SD,J}$) of key components; and finally, load fluctuations can also contribute to the degradation of system components. The effect of these factors is reflected as an increase in system downtime or increase in MTTF, reduced system reliability, and, in some cases, increased maintenance costs [37].

Numerous research indicates that the actual stresses (thermal, electrical, thermal cycling, mechanical, humidy and chemical), as well as induced over-stresses (placement, application, and ruggedizing) in the power semiconductor devices are the major causes of failure [14]. In response to this, various methods, both active and passive, have been suggested to alleviate these stress factors and delay the onset of aging-related failures. For example, passive thermal management strategies involve substituting components with those possessing greater resilience to stress. On the other hand, active thermal management concentrates on enhancing the converter's control unit to bolster reliability. Measures such as active and reactive power control, power distribution strategies, and other techniques aimed at mitigating thermal stress or effectively dispersing heat across components represent some of the active interventions pursued in this regard.

Amidst the various methods of improving the reliability of PEC systems, it is essential to identify the design parameters and determine the optimum combination(s)[2] that serves the objective of reducing/minimizing the system failure rate (FR) and, therefore, improving the overall downtime. This leads to the motivation for this research, which stems from the need to address the above mentioned challenges and explore how Genetic algorithm (GA) can be employed to optimize the objective functions.

While various techniques and methods for improving the reliability of converter systems exist,

[2]In some cases, as we shall later see, the design variables affect two or more of the design objectives, hence an observation of the Pareto frontier is necessary.

which can categorically be grouped under the umbrella of three major terms - "prognostics and health management," "active thermal control," and "fault-tolerant control" [22], this thesis focuses on the latter two in its problem formulation. These major categories are influenced by various parameters that contribute inter-relatedly and, in some cases, isolatedly to the reliability of the components that make up the PEC system. In light of these, optimization of these reliability improvement opportunities becomes a critical necessity of research and development, hence the focal point of this thesis.

Table 1.2: Failure and repair trends in wind turbines and HVDC systems [60].

Unit	**Subsystem**	**Component**	**Failure rate** [occ/y]	**Repair rate** [r/y]
WT	Converter (con.)	Switch	0.15	150
		Capacitor	0.2	150
		Other con. comp.	0.15	185
	Other	Other WT comp.	0.53	200
HVDC	Converter (con.)	Switch	0.3	200
		Capacitor	0.43	50
		Other con. comp.	0.35	10
	Other comp.	DC Line.	0.003	17

Another way of considering why this research is relevant is this: in the grand scheme of things, it seeks to answer the question: "Based on the many approaches and guidelines that have been proposed to predict aging failures considering uncertainties, what are the parameters that are within our control which when employed, provide the highest possible reliability/lifetime of the power electronic converter which then translates to a reduced system-level downtime?" It must be noted that some relevant models are solely focused on the failure rate, and the problem formulation in those cases becomes a minimization problem, whereas in other cases, the reliability is modeled after the lifetime or cycles to failure; hence, the problem formulation becomes one of maximization. Table 1.2 is referenced to show the impact of failure rate frequency of some power electronic devices in wind turbine (WT) and HVDC applications.

Before going in-depth, it might not be so apparent how complex the answer to the question can

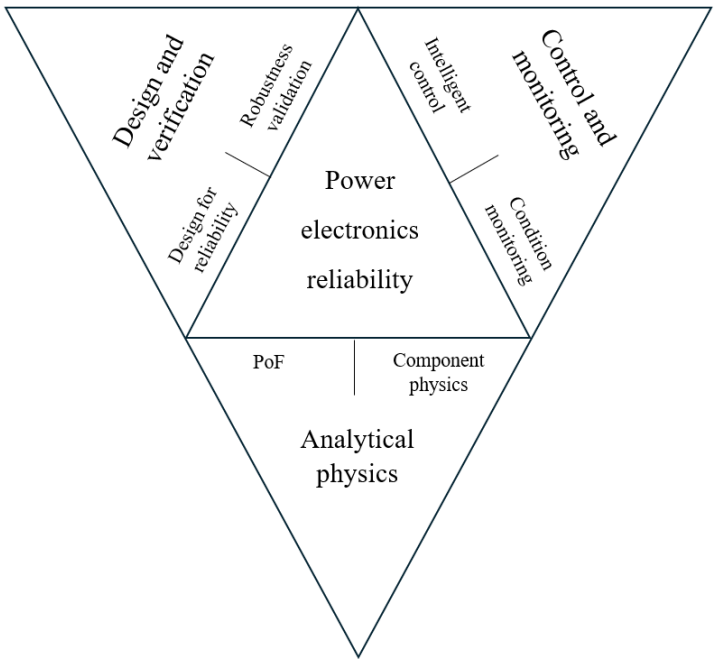


Figure 1.4: Modern power electronics reliability requirements [22].

be, especially when we consider the fact that the reliability is influenced by a myriad of parameters that are or are not interdependent. The bigger picture is best conveyed in Figure 1.4, which shows the inter-correlation of all necessary processes and considerations that must be satisfied to improve not only the reliability of any given PEC but also its efficient operation. While many parameters influencing the reliability/lifetime of any specific power electronic converter component can be altered to improve its reliability, it is worth noting that doing so by one or more of the control parameters might affect the reliability of other components. Another point of interest is that several of these parameters are outside a design engineer's control. In summary, there is no general answer that is applicable as a panacea for all power electronic converters since they all vary in terms of function, design, manufacturer, material type, component type, method of control, frequency of operation, physics of failure (PoF), etc. This point is depicted in Figure 1.4, which shows modern reliability requirements of PECs.

Figure 1.5 goes a step further to represent how the reliability problem can be observed from the component level. It can be seen that many components constitute any single PEC system, and each of these components contribute to the reliability of the overall converter. We shall see in the literature review chapter that much research has shown that the PEC components that are most susceptible/vulnerable to failure are the power semiconductor devices (including but not limited to

Si and SiC IGBT, MOSFET, GaN devices) and capacitors [59], [64], [70]. "They are considered as the reliability-critical components in PECs, especially the IGBT modules in medium to high-power applications and capacitors for AC filtering and DC-link applications" [22]. As a result, the problem formulation of this paper is centered mainly around these two components.

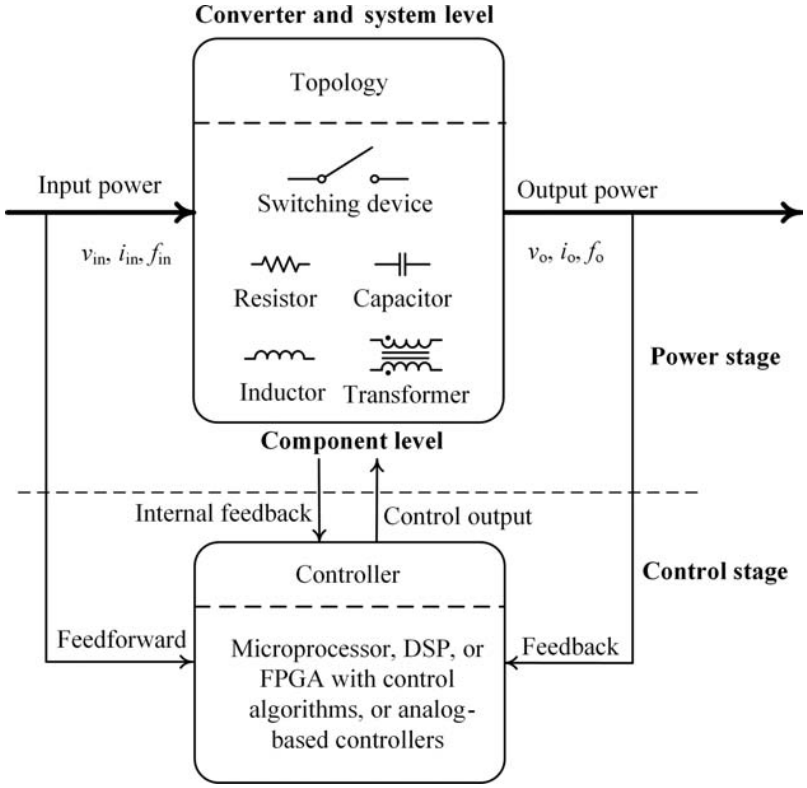


Figure 1.5: Architecture of a typical power electronic converter system [22].

Considering the switching frequency (f_{sw}) of the application, for instance, while controlling this parameter by reducing it has a positive impact on the reliability of the switching device in that the thermal effect is minimized; doing so also contradicts the purpose of miniaturization. Perhaps the size of the heatsink may be increased to accommodate and dissipate large amounts of power losses in the form of heat. But the question is how big[3] is enough? Maybe the system should be made to accommodate fault tolerance by considering component redundancies. Again, we are faced with the question of how many and how much[4] is enough?

In response to such challenging and contradicting PEC reliability influensors, the application of optimization techniques is considered a promising avenue for enhancing the reliability of PEC

[3]This is in reference to overall device size contraints.

[4]This is in reference to money contraints.

systems. Among these techniques, genetic algorithms (GA) have garnered considerable attention due to their ability to efficiently explore large solution spaces and identify optimal configurations [40],[71]. By leveraging the principles of natural selection and evolution, glsGA offer a unique approach to addressing the multifaceted optimization requirements of complex engineering systems.

This research direction not only underscores the increasing importance of reliability enhancement in PEC systems but also reflects a forward-looking integration of advanced computational methods. The synergistic combination of reliability improvement techniques and GA holds the potential to yield innovative solutions that can mitigate failure modes, enhance system resilience, and ultimately contribute to the sustainable and dependable operation of low, medium and high power systems that depend on power electronic converter systems.

Scientific contribution

The contribution section of this thesis highlights several significant advancements in the field of PEC reliability improvement techniques through the application of GA. In that regard, this thesis aims to make the following contributions:

1. The optimization of reliability improvement strategies of PECs, therefore addressing crucial downtime challenges in modern power systems. By leveraging GA, innovative solutions have been selected/devised to mitigate failure risks and enhance the overall reliability of power electronic systems.

2. The advancement of optimization methodologies by demonstrating the efficacy of GA in addressing complex optimization problems inherent in power electronics reliability improvement. The utilization of GA enables efficient exploration of solution spaces, leading to the identification of robust and optimal configurations for enhancing converter reliability.

3. Furthermore, this research significantly advances the understanding and application of genetic algorithms in optimizing power electronic converter reliability, providing valuable insights for future research and practical implementations in the power electronics industry.

Structure of this thesis

This thesis delves into the application of GA for optimizing the reliability improvement of PECs. Unlike traditional methods, this approach leverages the power of GA to evolve design configurations that prioritize enhanced reliability metrics like FR and MTTF. The core of this research lies in establishing a framework that seamlessly integrates GA with established space, encompassing factors such as component sizing, thermal management strategies, and control frequency. The GA is meticulously tailored to the specific PEC under investigation - in this case, the half-bridge inverter - with carefully crafted fitness functions that prioritize reliability improvement while ensuring adherence to desired performance benchmarks.

Chapter 1 laid the groundwork by introducing the concept of reliability in PECs and outlined how various factors tend to influence it. The chapter then delved into the application of GA as an optimization technique for improving PEC reliability. Furthermore, chapter 1 touched on the specific objectives of this research, outlining the scope of the project and acknowledging any limitations inherent to the chosen approach.

Chapter 2, under the literature review section, delves into the existing body of research on PEC reliability improvement, where a comprehensive review of various existing scholarly literature relevant to the topic of PEC reliability improvement is done.

Following the literature review, **Chapter 3** dives into the heart of this research: the methodology for optimizing PEC reliability improvement using GA. Here, the frameworks for the reliability of the critical components are determined and employed. The failure rate (FR) models are used to represent the random failure phase, whereas the lifetime models are used to represent the wear-out failure phase. Reliability improvement parameters and constraints are also identified. Single and multi-objective optimization problem formulations are then established.

In **Chapter 4**, the optimization results are presented. Analysis are made based on the optimum parameters and solutions identified by the genetic algorithm. Visualization plot including pareto frontier, parallel plots and scatter plots are employed to present the nuances in the results.

Finally, in **Chapter 5**, conclusions are presented. The key findings of the work are summarized. Finally, limitations and suggestions for further research are also presented.

CHAPTER 2

LITERATURE REVIEWS

Concept of reliability in power electronic converter systems

This literature review chapter will begin by examining the past as well as the current state of PEC reliability, their significance in various applications, and the challenges faced in enhancing their reliability. The chapter provides a comprehensive overview of the existing research and scholarship in the field of reliability improvement techniques for power electronic converters. By synthesizing and critically analyzing the relevant literature to understand the breadth and depth of research conducted in this domain, this chapter aims to establish the current state of knowledge, identify key trends and challenges, and pave the way for the research presented in this thesis. Subsequent sections will delve into the principles of GAs, their unique advantages in solving complex optimization problems, and how they have been applied to power electronics thus far.

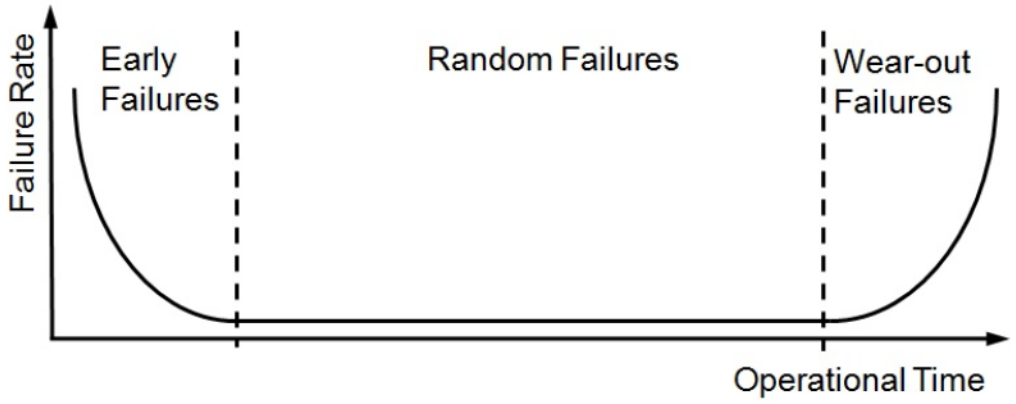


Figure 2.1: Failure diagram of electronic components and systems [1].

Reliability, defined as the ability of a system to consistently perform its intended function under specified conditions for a defined period [50], is a paramount concern in critical applications where downtime can lead to significant economic losses or safety risks [48],[64]. Consequently, in order to design and implement any reliable electrical system, it is essential to take into consideration possible potential interruptions due to power converters, the estimated load and demand on them, as well as the duration of such interruptions [24]. As such, the discussion of power electronic converter (PEC) reliability cannot be initiated without the mention of the "bathtub curve," which is a well-established graphical representation in reliability engineering that depicts the failure rate of a system over its

lifetime [15], [22], [34], [60], [69]. In the context of PEC systems reliability improvement, this curve holds significant relevance in the establishment of the optimization problem formulation as we will see in the methodology chapter. The curve is divided into three sections, as shown in Figure 2.1, where the initial phase of the represents early failures also known as "infant mortality" period, during which a higher rate of early failures is observed. The causes of these early failures can be attributed to various reasons ranging from manufacturing defects to design flaws and debugging processes [59]. This underscores the importance of robust design and manufacturing processes to mitigate these early failures [14]. The subsequent phase, referred to as the "random failures" phase, reflects a relatively constant or useful-life period, where the system operates with a low and steady failure rate. For this reason, while it is fairly cumbersome to mathematically and reliably represent the early failure phase, suficient models have been developed to represent the random failure phase for which the GA optimization technique is centered around to enhance the PEC's resilience and minimize this phase. Finally, the curve's third phase - the "wear-out" phase - represents the end-of-life period of the PEC, where the failure rate increases as the system ages. This phase is characterized by an escalating rate of failures due to wear and tear, component aging, and other factors associated with prolonged use. Eventually, the failure rate exceeds the level observed during the useful life phase, leading to the eventual retirement or replacement of the PEC.

It shall be seen in later sections that while the early failure phase provides very little degree of control in the system's lifetime, the random and wear-out failure phases are the two phases on which we can center the reliability improvement optimization problem. Furthermore, by employing some applicable lifetime models, the wear-out phase can be modeled after the lifetime, or cycles to failure depending on the relevant components, thereby contributing to the overall optimization of the PEC system's reliability. This approach provides the groundwork for defining the fitness functions that will be provided to the optimization algorithm to minimize the useful failure rate and maximize the lifetime or cycles to failure. All this is to underline the practical significance of the bathtub curve in guiding the reliability optimization efforts for PEC systems.

Hierarchical levels of reliability assessment

While failure records and surveys have shown that power converters represent the weakest link in such systems, compromising overall reliability, it is important to note that reliability estimation of

power electronic converters spans multiple levels, each with its own distinct focus and methodologies [2],[59]. In other words, assessing reliability in power converters involves a hierarchical approach, analyzing failure rates and mechanisms at three key levels: component, converter, and system [60], [62]. At the component level, reliability evaluation focuses on individual parts such as semiconductor devices, capacitors (Caps), and switching devices (SDs). This involves scrutinizing factors like manufacturing quality, material durability, and failure rates to ascertain the component's inherent reliability.

Moving up to the power converter level, the assessment encompasses the integration and interaction of components within the converter itself. Evaluations here, delve into the converter's operation, thermal management, and fault tolerance mechanisms, crucial for maintaining stable power conversion under varying conditions.

At the system level, reliability analysis considers the holistic performance of the entire system, including not only the power converters themselves but also their integration with other subsystems and external factors that constitute, say, the smart grid, an aircraft, or even an EV. Figure 2.2 is referenced as a representation of the three hierarchical levels.

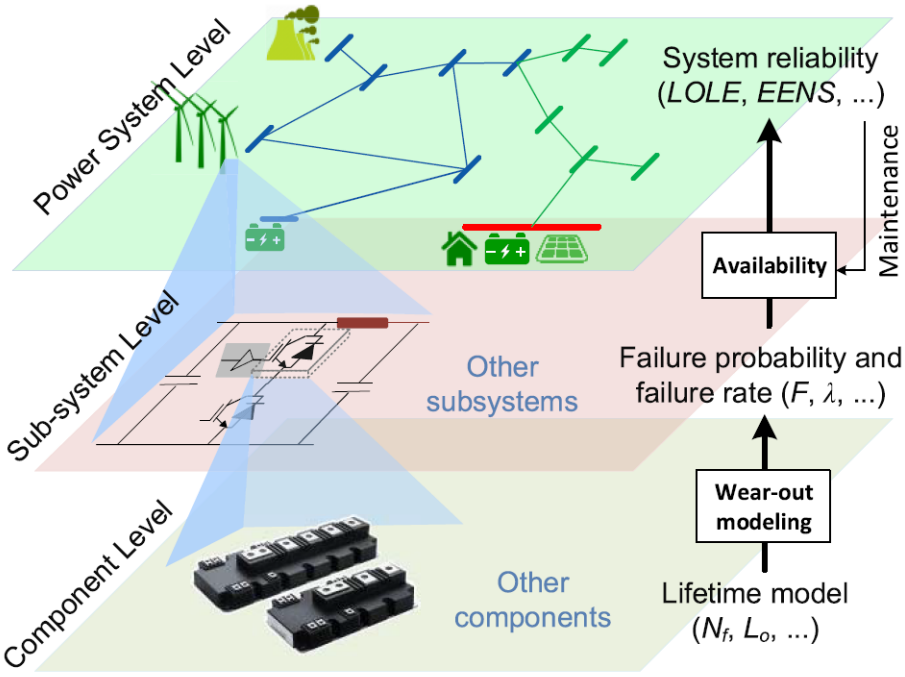


Figure 2.2: Hierarchical view of evaluating power converter reliability [60].

Hierarchical level 1 (component or device level)

The components (SDs, Caps, diodes, resistors, PCBs, etc.) are the building blocks of converters, and their reliability directly impacts the overall system reliability. Reliability assessment typically includes reliability models based on component stress factors, environmental conditions, and failure rates obtained from accelerated life testing and field data analysis. Datasheet specifications, lifetime estimations based on stress factors (temperature, voltage, current), and historical failure rates of these components are considered. Techniques such as Weibull analysis and reliability block diagrams are commonly employed to quantify the reliability of components and predict their failure probabilities over time.

Reliability assessment at the component level involves datasheet specfications, which provide a wealth of information about individual components. Maximum ratings define the voltage, current, temperature, and other operating limits that the component can handle without failure. Exceeding these limits can significantly accelerate degradation and shorten lifespan. Furthermore, the Physics-of-Failure (PoF) analytical approach delves into the underlying physical mechanisms that can lead to component failure. Common PoF mechanisms in power electronics include thermal cycling and dielectric breakdown. Moreover, derating factors such as multipliers applied to the maximum ratings to define the actual operating conditions below their maximum ratings is a crucial strategy to enhance reliability. Derating reduces stress factors like temperature and current density, leading to a longer component lifespan. Choosing component sizes with inherently higher reliability ratings and appropriate specifications for the application is important and must be carefully considered to achieve the optimum lifetime.

Hierarchical level 2 (subsystem or converter level)

Moving beyond the building blocks, the converter level, which encompasses the entire reliability of the power converter circuit, emphasis shifts from individual component failure rates to how components interact within the circuit and how circuit design choices influence overall converter reliability. In other words, reliability estimation involves integrating the reliability information of individual components and assessing the converter's overall performance and failure behavior. This involves modeling the interactions between components and understanding how design choices and operating conditions can lead to hardware random failures within the converter's useful life and

wear-out period [59], [61]. This includes analyzing the converter topology, control strategies, thermal management, and redundancy techniques to identify potential failure modes and their effects on system reliability. Methods such as fault tree analysis and reliability-centered maintenance are utilized to evaluate the reliability of the converter system and optimize its design for enhanced robustness and fault tolerance.

The chosen converter topology (e.g., buck, boost, buck-boost, half-bridge) can impact reliability depending on the number and type of failure-prone components are being used. This is in addition to the fact that factors like voltage stress on components, switching frequency requirements, and thermal management challenges vary depending on the topology, and a well-designed topology can minimize stress on components and improve overall reliability.

Implementing redundancy at the converter level involves using multiple components in parallel to achieve fault tolerance. In case of a single component failure, the remaining redundant components can take over the functionality and maintain converter operation, improving overall system reliability. However, redundancy adds control complexity, weight, and cost and requires careful design to ensure proper load sharing and fault detection/isolation. Enforcing appreciable constraints is, therefore, a necessity in order to determine the optimum combination of design choices. Also, the control strategy employed by the converter plays a significant role in reliability; a well-designed control system can ensure stable operation, minimize transient stresses on components, and respond effectively to potential faults. Conversely, a poorly designed control system can introduce instability or excessive stress on components, leading to reduced reliability.

Hierarchical level 3 (power system level)

At the power system level, reliability estimation extends beyond individual converters to consider the entire power generation, transmission, and distribution infrastructure. The system level takes the analysis beyond the confines of the power converter itself and considers its role within the broader system it serves. The focus shifts to how converters perform within larger networks such as transmission stations and power plants. Here, reliability is influenced by external factors like environmental conditions and system-level interactions [22]. In other words, this includes assessing the reliability of transmission stations, power plant stations, and grid interconnections to ensure continuous and stable power supply to end-users.

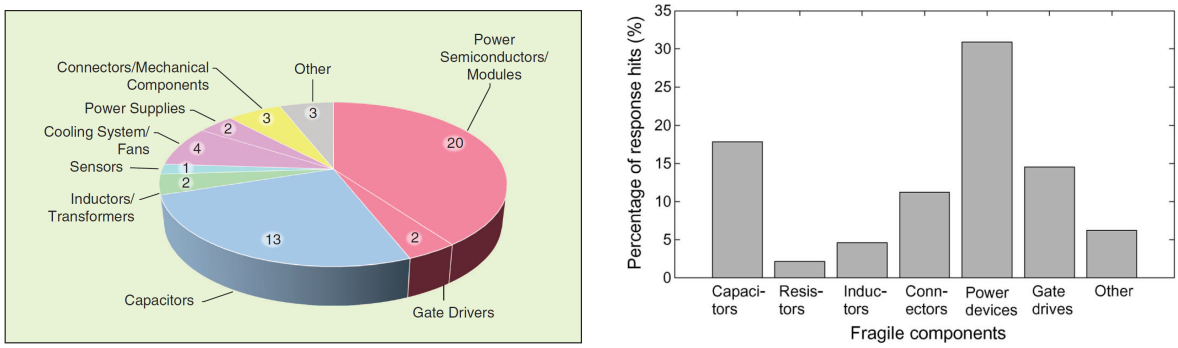
The operating environment of the system plays a crucial role, where factors like ambient temperature, humidity, vibration, and exposure to dust or contaminants can all affect the converter's reliability. Derating strategies and component selection might need to be adjusted based on the expected environmental conditions. Additionally, proper enclosure design and environmental control measures can be implemented to mitigate external stresses on the converter. Regular maintenance schedules/practices can significantly enhance system reliability. This includes periodic cleaning of the converter and passive thermal management components (heatsinks, fans) and monitoring component performance to identify potential issues before they escalate into failures. Furthermore, the way in which the converter integrates with other components in the system needs to be considered. Issues like inrush currents from loads, electromagnetic interference (EMI) from other devices, and potential ground loops can all impact the converter's operation and reliability. Because a failure within the converter can have cascading effects on other parts of the system, system-level analysis, which involves identifying potential cascading failure and implementing preventive measures like redundancy or fault isolation to minimize their impact, is essential. Since the system's required uptime might be mission-critical, redundancy strategies, component sizing, and maintenance schedules can all be adjusted/constrained based on the specific uptime requirements of the overall system.

Having made the above discussions, techniques such as reliability indices (e.g., LOLE, LOLP, EENS), Monte Carlo simulation, and system-wide fault analysis are employed to evaluate the reliability and resilience of power systems under various operating conditions, contingencies, and disturbances [5], [60]. By integrating reliability estimation across these three levels, from component to subsystem to power system, comprehensive insights can be gained into the overall reliability of power electronic converters and their impact on the reliability of the broader power infrastructure.

Identifying the failure-prone components in Power Converters

Power semiconductor devices (SDs) and electrolytic capacitors have been identified as the most fragile components susceptible to wear-out failure in PECs and emerge as the leading contributors to failures [23], [30], [42], [64]. This is reflected in industry surveys as shown in Figure 2.3 where SD makes up about 33% of the failure-prone components, and Caps make up about 25%. Whereas semiconductor switches experience stress due to high currents and rapid switching transients, leading to potential failure mechanisms like electromigration and thermal cycling, elec-

trolytic capacitors degrade over time due to factors like temperature and ripple current, eventually losing their capacitance or experiencing a dielectric breakdown. Furthermore, SDs such as IGBTs, MOSFETs, and diodes used in the inverter switching circuits experience thermal cycling and high electric fields during operation. This can lead to failure like bond wire lift-off, solder fatigue, and dielectric breakdown[1] over time [45].



(a) (b)

Figure 2.3: (a) The most important components requiring immediate address [12], [30]. (b) The most fragile components in a PEC [64].

Moreover, research also shows that electrolytic capacitors used for DC-link filtering and snubbers are also highly prone to degradation. The capacitance value decreases while the equivalent series resistance (ESR) increases due to the evaporation of the electrolyte over many thermal cycles. The effect of this is increased power losses, heating, and eventual failure of the Cap.

The failure mechanism of the critical components

Following the analysis above, it has been established that SDs and Caps form the foundation of the entire power system, and their reliabilities constitude a huge percentage of the system reliability. That is to say, the reliaibility and longevity of the entire network hinge critically on the performance and integrity of these key components. Not only are these elements pivotal in managing and regulating the flow of electrical currents, but their failure can lead to significant operational disruptions.

This section delves into the various factors that contribute to the degradation and eventual

[1] This is only the case in capacitors

failure of these components, exploring how their performance impacts the overall system reliability and what measures can be taken to mitigate these risks.

Power-switching device failure mechanisms

The reliability of SDs, like IGBTs and MOSFETs, is influenced by several factors, including material properties and operating conditions. A critical challenge arises from the coefficient of thermal expansion (CTE) mismatch between the various materials within any given SD module [21], [25], [44], [47]. The silicon (Si) die typically having a low CTE, expands at a different rate compared to the surrounding packaging materials like ceramic substrates - which typically have higher CTEs - and copper (Cu) baseplate (with even higher CTE) during power cycling. This mismatch creates significant thermal stress within the device. Over time, this stress can lead to fatigue and cracks in the solder joints that connect the die to the substrate, potentially compromising the electrical connectivity and heat transfer. Table 2.1 is referenced here for additional information.

Table 2.1: Typical thickness, CTE, and length of SD material composition [44].

Material	**t** (μm)	**CTE** (K^{-1})	**L** (mm)
Al	300	23×10^{-6}	1
Si	250	2.6×10^{-6}	12
Solder	100	24.5×10^{-6}	
Cu	280	16.5×10^{-6}	
Al_2O_3 or AlN	1000	7.0×10^{-6}	30 - 55
Cu or AlSiC	4000	7.5×10^{-6}	

Another prevalent failure mechanism is "bond wire lift-off." IGBTs utilize thin aluminum bond wires to connect the silicon die to the external terminals. The significant CTE difference between aluminum - with a high CTE - and the surrounding materials can cause these bond wires to experience excessive stress during thermal cycling. This stress can lead to the progressive weakening and eventual lift-off of the bond wire, resulting in open circuits and device failure. As such, careful control of operating temperatures can help mitigate such failure modes. Additionally, as suggested in [52], there exists a strong correlation between the bond wire sizing and the cycles to failure

(N_f). Hence, employing robust sizes and bonding techniques for the bond wires can enhance the SD resistance to thermal stress and extend its lifespan. Examples of the effect of bond wire lift-off are shown in Figure 2.4.

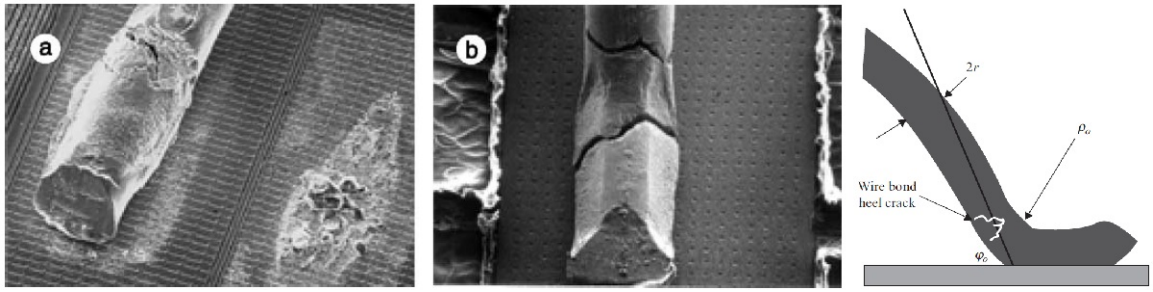


Figure 2.4: Different PoF mechanisms of bond wire failures [22], [44].

Although this thesis does not go into detail on the analysis of the components' reliability[2] but merely employs the PoF models developed to later establish the optimization problem formulation, it is worth describing the model that represents how the bond wire failure relates to the switchgin device's cycles to failure. This is given in the equation below.

$$N_f = A \cdot \varepsilon_f^n \tag{2.1}$$

$$\varepsilon_f = \frac{r}{\rho_0}\left(\frac{cos^{-1}(cos\varphi_0)(1-\Delta T\Delta\alpha)}{\varphi_0} - 1\right) \tag{2.2}$$

where A and n are constants for the bond wire material, and ε_f is the bond wire strain. $\Delta\alpha$ is the mismatch in the CTE between the aluminum bond wire and the Si. φ_0, ρ_0, and r are geometric parameters as defined in [22].

Without a doubt, failure modes such as the bond wire lift off are influenced by operating temperatures. This is seen in Figure 2.4 where higher temperatures increase the mobility of metal atoms with the material, exacerbating electromigration and accelerating the formation of voids that can lead to open circuits. Additionally, thermal cycling stress becomes more pronounced with larger temperature swings. The repeated expansion and contraction caused by these variations induce greater mechanical fatigue in the device materials, promoting crack formation and delamination.

[2]This work has already been done in [18].

This cumulative damage ultimately reduces the SD's lifespan and increases the risk of catastrophic failure. A typical thermal variation of a SD is shown in Figure 2.5 for reference. Where $T_{SD,J}$ is the chip temperature, and T_c is the baseplate temperature.

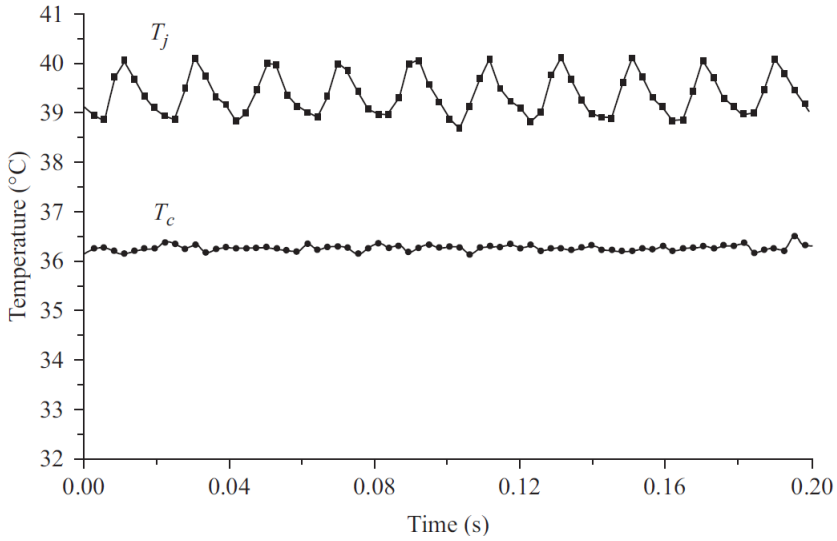


Figure 2.5: Temperature swing of on a 10-kW three-phase PV inverter [22].

Power capacitor failure mechanisms

Power capacitors, especially electrolytic capacitors used in DC-link applications of PECs, are prone to wear-out failures due to various key mechanisms, including electrolyte degradation, voltage stress, aging, oxide layer growth, and core corrosion, among other factors.

The main failure mechanism in power Caps has been identified as the gradual evaporation of the electrolyte liquid over time and thermal cycles. As the electrolyte evaporates, the capacitance value decreases while the equivalent series resistance (ESR) increases [3], [26]. This leads to increased power losses, heating, and eventual failure of the capacitor.

Another contributor to capacitor degradation is the growth of the oxide layer on the anode foil. This increases the distance that charge carriers must tunnel through, reducing the capacitance. Furthermore, the growth of the oxide layer is also accelerated by high temperatures.

Furthermore, ingress of moisture or contaminants can cause corrosion of the internal aluminum anode and cathode layers, leading to an increase in leakage current and eventual short circuit failure.

The wear-out failure rate of capacitors depends strongly on operating conditions like temperature, voltage, humidity, and ripple current [3], [14]. Whereas higher temperatures accelerate electrolyte evaporation, high voltages and ripple currents increase internal heating. The Cap's lifetime is estimated using physics-based models like the Arrhenius equation for temperature and inverse power law for voltage.

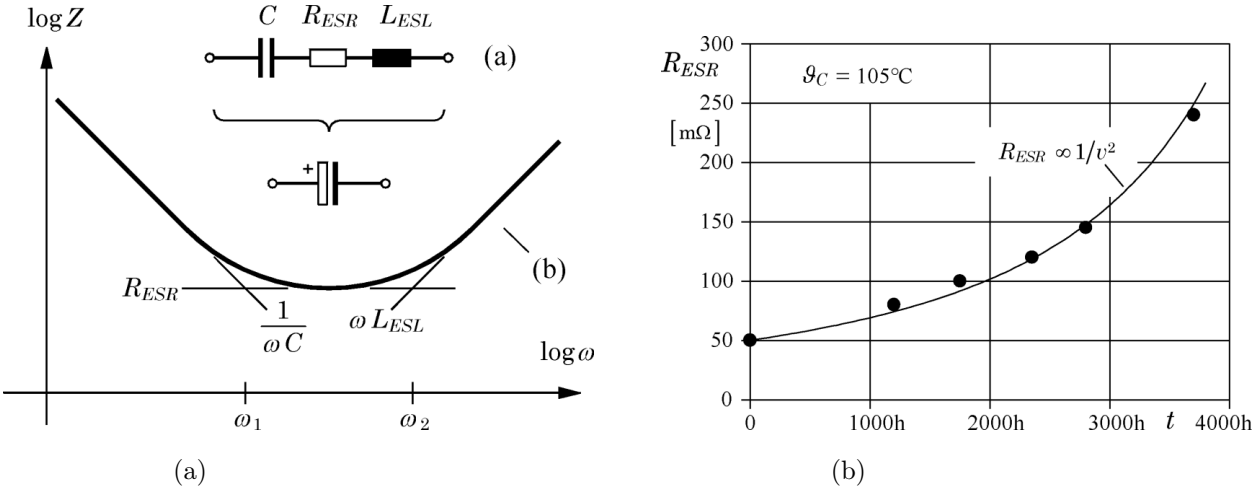


Figure 2.6: Electrolytic capacitor characteristics and failure factors [43].

The equivalent circuit diagram of an electrolytic capacitor is modeled using the following equation which constitutes the series connection of the capacitance (C), an ohmic resistor (R_{ESR}) that represents all ac losses, and a stray inductance (L_{ESL}) that depends on the winding design and connection of the Cap foils to the terminals [43].

$$Z_C(s) = R_{ESR} + sL_{ESL} + \frac{1}{sC} \tag{2.3}$$

The parameters that influence the above occurrences are the frequency of operation and the duration of operation, as shown in Figure 2.6. Making reference to the figure, it has been shown that increased ESR to around 30% or 40% is a pretty good indication of a capacitor's end-of-life.

Reliability improvement techniques of power electronic converters

We have looked at the failure modes/mechanisms of PECs at all hierarchical levels. We have also established that failure at the component level are what lead to a cascading effect and eventual failure at the sytems level. At this point, we now turn our attention to some of the strategies that

have been deviced to mitigate these failure modes.

According to [22], [59], and [64], the reliability improvement of PECs can generally be categorized under the following three terms.

- Prognostic and health management (PHM)
- Active thermal control (ATC)
- Fault-tolerant control (FTC)

Prognostic and health management strategy (PHM)

PHM involves monitoring the health state of critical components and predicting their remaining useful life through physics-based degradation models and data-driven techniques. In this strategy, on-state voltage monitoring and current/temperature sensing can track the degradation of power devices due to mechanisms like bond wire lift-off and solder fatigue [23]. Similarly, capacitance and dissipation factor measurements can detect electrolyte evaporation and oxide growth in DC-link capacitors.

The monitored parameters are then mapped to an estimated remaining useful life using PoF models like the modified[3] Arrhenius equation for temperature effects or empirical models derived from accelerated aging data. This enables condition-based maintenance by triggering capacitor replacement or allowing graceful degradation of converters before catastrophic failures occur. The idea behind PHM as applicable in PECs can even be taken a step further via the employment of artificial neural network (ANN) [18], [58].

Effective PHM strategies allow for optimizing converter operation within thermal and electrical limits, extending maintenance intervals, and improving the overall reliability and availability of power electronic systems. A downside or rather, a challenge in this approach is that, PHM strategies require robust sensors, data acquisition systems, and validated degradation models for implementation.

[3]Here, I use the term "modified" loosely to make reference to the acceleration factors when employing the FIDES approach

Active thermal control (ATC)

Being one of the effective strategies for improving the reliability of PEC systems by regulating temperature and thermal cycling of critical components like power SDs and Caps, the key idea behind ATC is to actively manipulate the losses generated within the converter by adjusting control parameters like switching frequency (f_{sw}), modulation index (m), and current limits [29], [32], [41], [42], [51]. This allows regulating the junction temperature swing ($\Delta T_{SD,J}$) and mean junction temperature ($T_{SD,J}$) of SDs, which are the critical variables governing their lifetime from failure mechanisms like bond wire lift-off, solder fatigue, and dielectric breakdown [27], [28], [55], [66].

For example, reducing f_{sw} lowers the switching losses (E_{sw}) and $\Delta T_{SD,J}$, extending the power cycling capability [6]. Similarly, electrolytic capacitor degradation from electrolyte evaporation can be slowed by limiting the hotspot temperatures through active thermal management. PoF models like the modified Arrhenius equation relate these thermal stresses to the remaining useful life of components. A typical active thermal control strategy is shown in Figure 2.7, where the junction temperature of the most stressed SD is employed as the control parameter for the PEC. Here, the junction temperature influences the switching frequency that is used by the PWM controller.

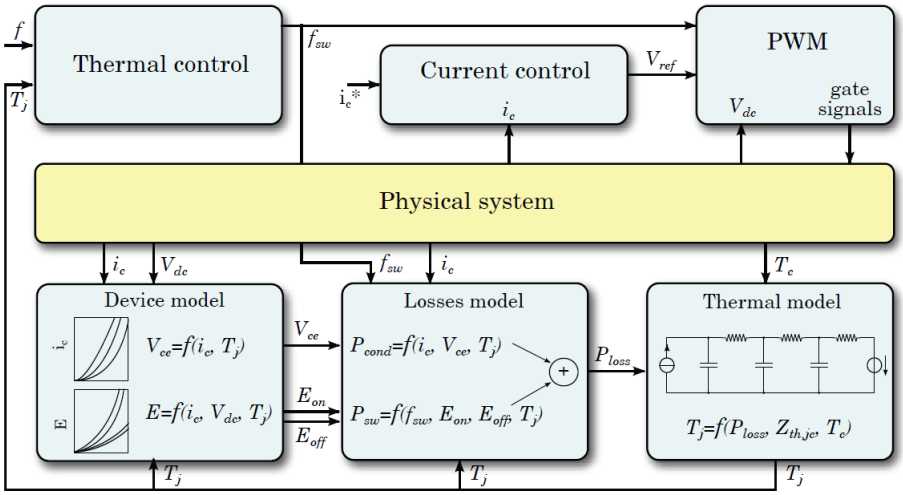


Figure 2.7: Example block diagram of a thermal control system [29].

Fault-tolerant control (FTC)

FTC is also an effective strategy to enhance the reliability of power electronic converter systems by enabling continued operation after the occurrence of faults in critical components like

power semiconductor devices or capacitors. The idea here, is to reconfigure the converter control and modulation strategy to bypass or compensate for the faulted components, allowing the system to operate at a degraded but acceptable level [8], [10], [38]. This prevents complete shutdown and improves overall availability.

"Five main fault examples are identified as single-switch short-circuit (where the power semiconductor is de-saturated, and working as a current source or has a physical short circuit), phase-leg short-circuit, single-switch open-circuit, single-phase open-circuit, and intermittent gate-misfiring" [22]. For example, if an open-circuit fault occurs in one of the power switches, the faulty switch can be bypassed by modifying the converter switching sequences and redistributing the load current among the remaining healthy devices. Similarly, faults in capacitors can be handled by rebalancing the voltages across the remaining capacitors through control actions. Figures 2.8 are examples of half-bridge NPC converter topologies modified for fault tolerance.

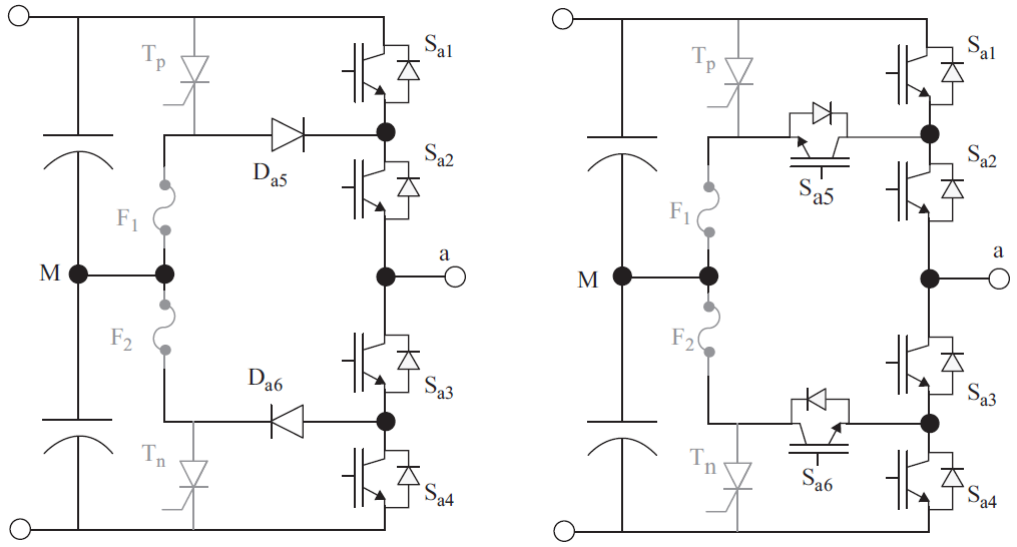


Figure 2.8: (a) Half-bridge NPC topology modified for fault tolerance, (b) Active-NPC topology modified for fault tolerance [22].

FTC strategies can be broadly classified into hardware redundancy[4] methods that use spare components, switching state redundancy that omits faulty states, and unbalanced compensation techniques. Advanced model-based controllers and optimization algorithms are employed to define

[4]Due to the mathematical complexity involved in modeling the other two methods, this thesis focuses on this method of FTC, specifically, parallel redundancy - as we shall see later on in the methodology chapter.

the optimal post-fault operating point and control actions [63]. However, fault-tolerant control requires robust fault detection and isolation schemes, as well as detailed converter models and constraints to ensure stable post-fault operation without violating device limits. However, it has been shown to be an effective means of extending the operating life of converters and preventing catastrophic failures.

Reliability requirements of power electronic converter systems

From the above discussion, it can be inferred that modern applications of power electronic converters continue to see a trend in device miniaturization; electrical, thermal, and mechanical performance; as well as feasibility. This is summarized in the following Table 2.2.

Table 2.2: Key factors for designing power electronic packaging [72].

Design considerations	**Details**
Size	Volume, weight, power density, energy density.
Electrical performance	Current rating, voltage rating, switching frequency, electromagnetic interference (EMI).
Thermal management	Temperature distribution, thermal resistance ($R_{SD,th}$), heat capacity, coefficient of thermal expansion (CTE).
Mechanical strength	Thermal stress distribution, material properties (Tensile strength, flexural strength, peel strength, etc.), external shock and vibration.
Reliability and fatigue	Joints failure, crack propagation, delamination, lifetime under temperature and power cycling.
Manufacturability and assembly	Manufacture procedure, process temperature and pressure, external connections.

In other words, PECs have gained stringent reliability requirements, especially for critical applications like renewable energy, industrial drives, and power transmission and distribution. As such, high reliability with a failure rate of less than 1% over the entire service life of $20 - 30$ years is ex-

pected for converter systems in WTs, photovoltaic (PV) plants, and HVDC transmission links. For industrial motor drives and automotive applications, a lower failure rate of around 5% is acceptable over a $10 - 15$ year lifetime [30], [64].

The MTTF requirement ranges from 50,000 hours for low-power converters up to 500,000 hours for multi-megawatt systems used in renewable power plants. Converters in safety-critical applications like aviation and medical equipment demand even higher MTTF values exceeding 1 million hours [30]. Fault detection and fault-tolerant operation capabilities are highly desired, allowing the system to operate through certain faults without complete shutdown. Condition monitoring and predictive maintenance features to schedule servicing before failures occur are also preferred for reducing downtime [22], [61]. Therefore, the reliability targets in terms of low failure rates, long MTTF values, fault tolerance, and predictive maintenance capabilities are very stringent for PECs, especially in renewable energy and high-voltage transmission applications, due to their critical nature.

Challenges in power electronics reliability improvement

Improving the reliability of power converters while pursuing other avenues such as miniaturization, cost, and safety, among other factors, faces several key challenges related to thermal management, switching losses, and associated costs. For instance, reducing the switching frequency is a common approach to lowering switching losses and improving efficiency, but it necessitates larger magnetic components like inductors and transformers, limiting miniaturization potential. Conversely, increasing the switching frequency enables the use of smaller magnetics but leads to higher switching losses and more stringent cooling requirements.

Furthermore, effective heat dissipation is crucial for reliable high-density converter operation. Conventional air-cooled heat sinks occupy significant volume and area, restricting the degree of achievable miniaturization. Advanced cooling techniques like liquid cooling enable higher power densities but increase system complexity, cost, and potential failure points.

From a cost perspective, the use of wide bandgap semiconductor devices like SiC and GaN facilitates higher switching frequencies, temperatures, and thus miniaturization. However, these devices are currently more expensive than their Si counterparts [61]. Similarly, advanced packaging

techniques like integrated power modules improve power density but involve higher manufacturing costs. Furthermore, implementing prognostics and health management strategies for enhanced reliability requires robust sensors, data acquisition systems, and validated degradation models, adding further complexity and cost.

Since the key challenges involve optimally balancing the trade-offs between switching frequency, component sizing, thermal management approach, semiconductor technology, PHM, ATC or FTC implementation, and overall system cost to achieve the desired reliability targets simultaneously, this work seeks to employ GA to achieve this. It is important to note that the efficacy of other evolutionary algorithms have been proven to be sufficient in similar PEC single objective optimization requirements as was the case in the work done in [56] and other controller designs. In other words, one main reason GA was selected as the optimization algorithm of choice in this thesis is due to its ability to excel at handling problems with multiple objectives, as will be explored in the methodology section.

CHAPTER 3

METHODOLOGY

The chapter outlines the methodology used to optimize the reliability of the power electronic converter (PEC) system, in this case, the Half-Bridge Converter, through the application of Genetic Algorithm (GA). This section details the research design, data collection methods, model development/employment, GA implementation, and validation processes. The research follows an experimental design with simulation-based optimization. This involves employing a mathematical model of the reliability of the PEC's key components, defining their reliability metrics, and applying GA to optimize these metrics.

Half-Bridge Converter configuration

The half-bridge converter is a type of DC-DC converter that is commonly used in power electronics applications for converting a DC input voltage to a DC output voltage. This is converter is known for its efficiency and ability to handle high power levels, making it suitable for applications such as power supplies, inverters, and motor drives.

The converter consists of two main power-switching devices (typically MOSFETs or IGBTs) and two capacitors. The basic structure includes two SDs (Q_1 and Q_2) connected in series across the input DC voltage source. The midpoint between the switches serves as one of the AC outputs. Two diodes are sometimes connected in parallel across the switches to provide freewheeling paths for the current when the switches are turned off. Two capacitors (C_1 and C_2) are also connected in series across the input voltage source, providing a mid-point voltage reference and stabilizing the voltage across the switches. Figure 3.1 shows a basic configuration of the converter.

Half-bridge converter operating principle

The converter operates by alternately switching $IGBT_1$ and $IGBT_2$, which creates a square wave voltage at the midpoint between the switching devices. This voltage is then filtered to produce the desired AC output. The basic operating phases are described below:

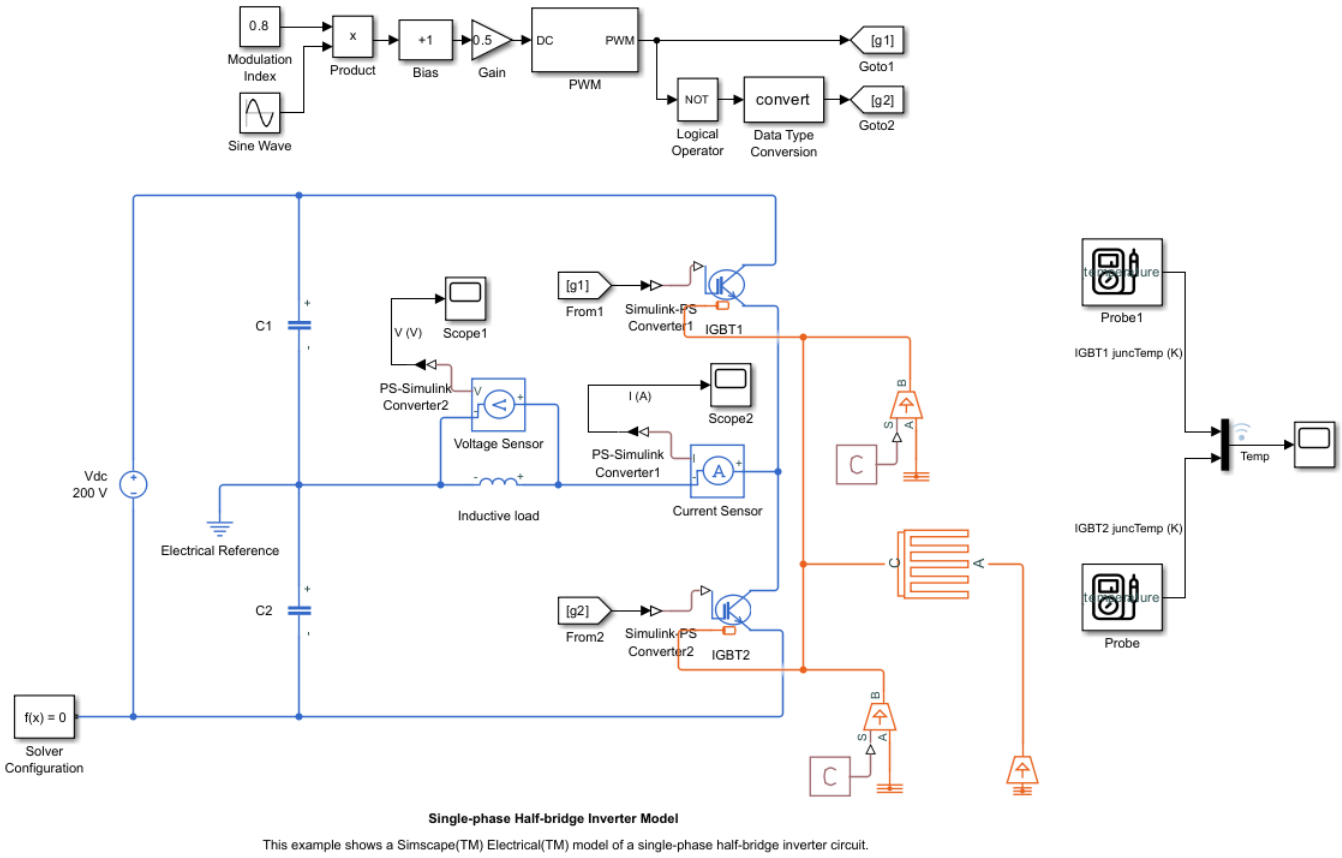


Figure 3.1: Half-Bridge converter configuration.

- **Phase 1 ($IGBT_1$ ON, $IGBT_2$ OFF):** When $IGBT_1$ is turned on and, $IGBT_2$ is off, the input voltage is applied across the load through $IGBT_1$ and C_2. During this phase, current flows from the input through $IGBT_1$ goes through the transformer to the load and returns via C_2.

- **Phase 2 ($IGBT_1$ OFF, $IGBT_2$ ON):** When $IGBT_1$ is turned off, and $IGBT_2$ is turned on, the input voltage is applied across the load through $IGBT_2$ and C_1. The current flows from the input through C_1 goes through the transformer to the load and returns via $IGBT_2$.

Reliability modeling of the converter

As shown in the literature review section, the total reliability at the power system level depends on the reliability at the components level. With that in mind, the problem formulation is targeted at the component level. Without much control over the infant mortality phase, the goal here is to optimize the reliability improvement techniques of the PEC, where the reliability is

a function of the failure rate (FR) and the failure rate of a device - in this case, a converter - is obtained as "the weighted average of failure rates in different operating phases" [11], [14], [53], [59]. It is given below in (3.2).

$$R_{PEC} = f(\lambda_{PEC}) \tag{3.1}$$

where

$$\lambda_{PEC} = \lambda_{PEC,useful} + \lambda_{PEC,wear} \tag{3.2}$$

$$\lambda_{PEC,useful} = \sum \lambda_{Caps,useful} + \sum \lambda_{SD,useful} \tag{3.3}$$

$$\lambda_{PEC,wear} = \sum \lambda_{Caps,wear} + \sum \lambda_{SD,wear} \tag{3.4}$$

where λ_{PEC} represents the total FR of the power electronic converter, $\lambda_{PEC,useful}$ is the useful FR that models the random/constant phase, $\lambda_{PEC,wear}$ is the wear-out FR. $\lambda_{Cap,useful}$, $\lambda_{SD,useful}$, $\lambda_{Cap,wear}$, and $\lambda_{SD,wear}$ are the Cap's and SD's useful FRs, and wear-out FRs, respectively.

Provided, we know the FR of the converter, the reliability in a given period (T) can then be determined using (3.5) below.

$$R_{PEC} = exp\left(-\int_0^t \lambda_{PEC}(T)dt\right) \tag{3.5}$$

The FIDES approach to failure rate prediction

The useful failure rate[1] of the power electronic component is best modeled after the FIDES guide approach, which offers a distinct approach to reliability prediction for electronic equipment. Unlike traditional methods that are heavily reliant on statistical analysis of historical data, the FIDES approach leverages the principles of PoF. This method considers the physical mechanisms that cause component failures under various stresses like temperature and electrical loads. The FIDES guide also integrates data from test results and field returns[2], particularly relevant for demanding environments like aerospace and defense. This combined approach aims to deliver a more realistic assessment of reliability, especially for cutting-edge technologies where historical data might be limited.

[1] This is the same as the random failure rate.

[2] Mission profile.

General model for predicting failure rate

The failure rate of an equipment is described using the following equation (3.6). Where λ_{Phy} is an additive expression of the physical and technological factors that contribute to the equipment reliability. Π_{PM} and $\Pi_{Process}$ are the multiplicative expressions representing the impact of development, production, and operating processes on reliability. Specifically, Π_{PM} is an expression of the quality and technical control of the equipment's manufacturing, while $\Pi_{Process}$ is an expression of the quality and technical control of the development, manufacturing and operating processes of the system[3] containing the equipment.

$$\lambda = \lambda_{Phy} \times \Pi_{PM} \times \Pi_{Process} \tag{3.6}$$

where

$$\lambda_{Phy} = \left[\sum_{Physical factors} (\lambda_0 \times \Pi_{Acceleration}) \right] \times \Pi_{Induced} \tag{3.7}$$

It is important to note that whearas little to no control can be had over the infant mortality period, the FIDES approach factors the infant mortality period into its model via the $\Pi_{Induced}$[4], Π_{PM}, and $\Pi_{Process}$ terms as will be seen later. For this reason, the remaining work done in this research assumes the best control processes. In other words, "best QA, RA, and ε" [supplier superior/under control ($Part\_Grade = 1$)], "all design rules are applied" ($Process\_Grade = 1$), and "all applicable recommendation practices are applied" ($Recom\_Grade = 1$), to ensure minimum impact from factors influencing the early failure fate period.

Modeling the early failure rate

The part-manufacturing (Π_{PM}), $\Pi_{Process}$, and $Pi_{Induced}$ expressions are given in (3.8) through (3.10).

$$\Pi_{PM} = e^{\delta_1(1-Part\_Grade)-\alpha_1} \tag{3.8}$$

$$\Pi_{Process} = e^{\delta_2(1-Process\_Grade)} \tag{3.9}$$

$$\Pi_{Induced} = (\Pi_{Placement} \times \Pi_{Application} \times \Pi_{Ruggedizing})^{0.511ln(C_{Sens})} \tag{3.10}$$

[3] Here, it could be a PEC when analyzing a SD or Cap. Or it could be an EV when analyzing a PEC.

[4] Specifically, in the $Pi_{Ruggedizing}$ term.

and

$$\Pi_{Ruggedizing} = e^{0.7(1-Recom\_Grade)} \tag{3.11}$$

where δ_1 and α_1 are the correlating factors that determine the size of the impact of Π_{PM}. δ_2 is the correlating factor that determines the range of variation of $\Pi_{Process}$. $Part\_Grade$ is the term that models the sum total of the manufacturer's QA, the equipment's QA and RA as well as the buyer's confidence level in the particular supplier (ε). $Process\_Grade$ is the score that reflects the level of process control on the equipment's reliability. $Recom\_Grade$ is the weighted recommendation score assigned to the equipment, which will be discussed further later on.

Table 3.1: Constants employed for the early failure rate modeling [14].

Constant	**Value**	**Constant**	**Value**
δ_1	1.39	Part_Grade	$[0-1]$
δ_2	2.079	Process_Grade	$[0-1]$
α_1	0.69	Recom_Grade	$[0-1]$
		C_{Sens}	6.30 (SD), 6.70 (Caps)

Induced/Overstress factors

Making reference to (3.10), the induced factors can be generally categorized into electrical overstress (EOS), mechanical overstress (MOS), and thermal overstress (TOS) origins [14]. Where $\Pi_{Placement}$ is the factor that represents the influence of the device's function in the system (in this case, the power converter), $\Pi_{Application}$ is the factor that represents the influence of the environment in which the converter operates, and C_{Sens} is a weight term representing the relative sensitivities of the overstress factors on the device.

For a given converter, C_{Sens} is calculated with the following equation, and assumed to follow the data in Table 3.2 based on the dedicated study on the behalf of the French MoD [14].

$$C_{Sens} = \alpha \cdot EOS + \beta \cdot MOS + \gamma \cdot TOS \tag{3.12}$$

where α, β, γ are the weights assigned to the EOS, MOS, and TOS respectively. The constants employed for the problem formulation as pertaining to C_{Sens} are given in [14].

The $\Pi_{Placement}$ parameter, as indicated in [14] must be assigned according to the electronic function served by the component (SD or Cap), and not according to the nature or technology of the component itself. Table 3.3 below shows the values assigned for each function that the SD serves. It is worth noting that this paper assumes the power analog interface function for high-power applications (thus, $\Pi_{Placement} = 2.5$).

Table 3.2: Values assigned for each potential function of a component [14].

Function	$\Pi_{Placement}$
Digital non-interface function	1.20
Digital interface function	1.60
Low-level analog non-interface function	1.30
Low-level analog interface function	2.00
Power analog non-interface function	1.60
Power analog interface function	2.50

The $\Pi_{Application}$ parameter, on the other hand is estimated from a check list and check sheet using an audit. This assessment as done through an evaluation, is graded into three levels, representing favorable, moderate, and unfavorable. A weight is then appropriately assigned to the corresponding condition. The equation below is used to estimate the $\Pi_{Application}$ factor of the component.

$$\Pi_{Application} = \frac{1}{66} \cdot \sum_{k=Criteria} W_{scores_k} \times W_{OS_k} \tag{3.13}$$

where W_{scores_k} is the weight assigned to each score/level, as shown in Table 3.3 below, and W_{OS_k} is the weight assigned to each overstress condition. The work done in [14] goes into much details about W_{OS_k} and shows that the criterion with the maximum weight is the user-related risk, followed by the product handling criterion. As such, these criteria have the highest impact in terms of contribution to the failure rate (λ) of the component.

The $\Pi_{Ruggedizing}$ similar to the $\Pi_{Application}$ is estimated from an audit/questionnaire that seeks to answer the following four questions to determine the level of compliance that goes into the manufacturing of the component:

- $L1$ = Recommendation not applied $\rightarrow$ Definite risks with regard to reliability

Table 3.3: Weights assigned to each condition for estimation of the $\Pi_{Application}$ [14].

Level	W_{scores}
0: Favorable	1.00
1: Moderate	3.20
2: Unfavorable	10.00

- $L2$ = Recommendation partially applied → Potential risks with regard to reliability
- $L3$ = Recommendation generally applied → Few risks with regard to reliability
- $L4$ = Recommendation applied fully and proceduralized → Reliability is under control

where the weights assigned to $L1 - L4$ are defined in Table 3.4 below, and each recommendation is weighted by a specific recommendation weight. Details on the weights pertaining to each recommendation are given in [14] and not discussed here. The expression for $Recom\_Grade$ is estimated using the following equation.

Table 3.4: Weights assigned to each level of recommendation for the $\Pi_{Ruggedizing}$ [14].

Level	**Score**
L1	0.00
L2	1.00
L3	2.00
L4	3.00

$$Recom\_Grade = \frac{1}{255} \cdot \sum_{i}^{Recommendations} (Recom\_Weight_i \times Satisfaction\_Score_i) \tag{3.14}$$

where $Recom\_Weight$ is the weight associated with a recommendation, and $Satisfaction\_Score$ is the score obtained for the corresponding recommendation. The $Recom\_Grade$ factor ranges from 0 (signifing worst case: no recommendation applied) to 1 (best case: all recommendation applied), while the $\Pi_{Ruggedizing}$ ranges from 1 (best case) to 2 (worst case).

Employing the the above constants in Table 3.1 through Table 3.5, Figure 3.2 plotted in "MATLAB" shows how the early failure rate is impacted by the manufacturing and control process. It can be inferred from the figure that all three factors have differing magnitudes of influence on the failure rate, with $\Pi_{Process}$ having the most impact, followed by Π_{PM} and finally, $\Pi_{Ruggedizing}$.

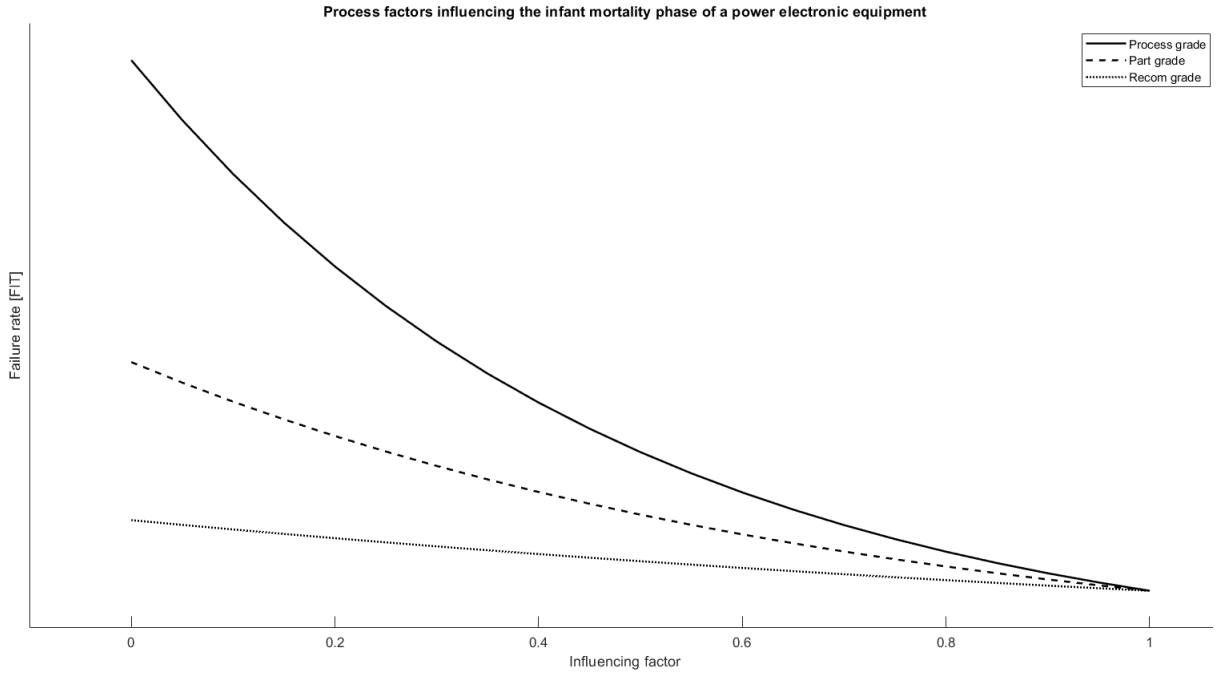


Figure 3.2: Process factors influencing the infant mortality phase of a power electronic equipment.

Modeling the useful failure rate of the SD

In contrast to the wear-out failure rate of the IGBT, which is modeled after the remaining lifetime[5] of the SD - which is later expanded on in later sessions - the useful failure rate, also known as the random failure rate, is prevalent during the equipment's operation. With reference to (3.6) through (3.11), the FIDES approach is adapted to model the useful failure rate of the SD and is given here:

$$\lambda_{SD} = \lambda_{SD,Phy} \times \Pi_{SD,PW} \times \Pi_{SD,PM} \times \Pi_{SD,Process} \tag{3.15}$$

$$\Pi_{SD,PW} = e^{\delta \cdot (1 - Process\_Grade) - \alpha} \tag{3.16}$$

where $\Pi_{SD,PW}$ is an acceleration factor (AF) related to the impact contributed by the SD's development. $\delta = 3.401$ and $\alpha = 0$ are the correlating factors that determine the size of the impact of

[5]Cycles to failure.

$\Pi_{SD,PW}$ on the SD's reliability.

Physical stress factors that impact the SD's failure rate

As mentioned earlier, the sum of the physical factors that impact a component's random failure rate make up the λ_{Phy}. In the case of the SD, (3.7) becomes:

$$\begin{aligned}\lambda_{SD,Phy} = \sum_{i}^{Phases} \left(\frac{t_{phase}}{T_{annual}}\right) (&\lambda_{0TH}\Pi_{Thermal} + \lambda_{0TCyCase}\Pi_{TCyCase} \\ &+ \lambda_{0TCySolderJoints}\Pi_{TCySolderJoints} + \lambda_{0RH}\Pi_{RH} \\ &+ \lambda_{0Mech}\Pi_{Mech})_i(\Pi_{Induced})_i\end{aligned} \tag{3.17}$$

where i is the index of the relevant phase [specification, manufacturing (design, board/assembly, equipment integration, system integration), operation, and maintenance] [14]. t_{phase} is the duration of the 'i'th phase within one year. T_{annual} is the number of hours in a single year, λ_{0TH} is the basic failure of rate the SD due to thermal contribution. $\Pi_{Thermal}$ is the acceleration factor indicating thermal stress sensitivity on the SD during its operation. $\lambda_{0TCyCase}$ is the basic failure of rate the SD due to thermal cycling contribution. $\Pi_{TCyCase}$ is the acceleration factor indicating thermal cycling stress sensitivity on the SD during its operation. $\lambda_{0TCySolderJoints}$ is the basic failure rate of the SD due to the contribution of the thermal cycling effect on the soldered joints of the SD. $\Pi_{TCySolderJoints}$ is the acceleration factor indicating thermal cycling stress sensitivity on the SD's soldered joints. λ_{0RH} is the basic failure rate of the SD due to the contribution of the relative humidity of the environment. Π_{RH} is the acceleration factor indicating relative humidity stress sensitivity on the SD during its operation. λ_{0Mech} is the basic failure rate of the SD due to mechanical stress contribution, and Π_{Mech} is the acceleration factor indicating the SD's sensitivity to mechanical stress during its operation. $\Pi_{Induced}$ is the contribution of the induced factors (overstresses) that are inherent to a particular field of application[6].

The complexity of the problem formulation is made apparent due to the dependence of $\lambda_{SD,Phy}$ on not only the relevant phase ('i') of the SD's application but also on the environmental factors and material type, as well as possible vibrations that go beyond the control of the designer. For these reasons, the assumptions made earlier are applicable in an attempt to minimize the mathematical

[6] $\lambda_{0TH}, \lambda_{0TCyCase}, \lambda_{0TCySolderJoints}, \lambda_{0RH}$, and λ_{0Mech} are sometimes provided in the manufacturer reliability datasheet

complexity of the problem formulation. Furthermore, the FR of the SD is considered only in the operation and maintenance phase (thus, $i = 1$). It is also assumed that a discrete high-power semiconductor, SMD, large heatsink, lead, and plastic type of SD is considered. The above assumptions translate to specific basic failure rates as provided in [14].

With the above assumptions, (3.17) is rewritten here as (3.18).

$$\begin{aligned}\lambda_{SD,Phy} = \left(\frac{t_{phase}}{T_{annual}}\right)(&\lambda_{0TH}\Pi_{Thermal} + \lambda_{0TCyCase}\Pi_{TCyCase} \\ &+ \lambda_{0TCySolderJoints}\Pi_{TCySolderJoints} + \lambda_{0RH}\Pi_{RH} \\ &+ \lambda_{0Mech}\Pi_{Mech})(\Pi_{Induced})\end{aligned} \tag{3.18}$$

Five physical factors are considered in the PoF modeling of the SD's FR. They are appropriately categorized in [14] as shown in table 3.6 below. In contrast to the induced stresses and the stresses developed from process factors, the physical factors are additive as mentioned earlier. It should be noted also that the thermal and electrical stress factors (Π_{Th}, Π_{Elec}) are usually categorized in combination as $\Pi_{Thermo-electrical}$.

Table 3.5: Physical stress factors applied to the product during its operational use [14].

AF	**Category**	**Description**
Π_{Th}	Thermal	Acceleration factor due to thermal influence
Π_{Elec}	Electrical	Acceleration factor due to electrical influence
Π_{TCy}	Thermal Cycling	Acceleration factor due to thermal cycling influence
Π_{Mech}	Mechanical	Acceleration factor due to mechanical influence
Π_{RH}	Humidity	Acceleration factor due to relative humidity influence

Effect of relative humidity on the SD's failure rate

SDs often rely on encapsulating materials like epoxy or silicone gel to protect the internal conmponents from the environment. High-humidity environments can cause these materials to absorb moisture. Over time, the moisture absorption causes degradation of the insulating properties of the encapsulation, potentially leading to increased leakage currents and reduced blocking capability

of the IGBT. This process weakens the overall reliability and can contribute to failures, particularly when the IGBT is already under thermal stress.

A modification to the Arrhenius equation is used to model the impact of relative humidity on the SD's failure rate. The formula is given in the following equation.

$$\Pi_{RH} = \left(\frac{RH_{amb}}{RH_0}\right)^{4.4} \cdot e^{\frac{E_{SD,a}}{K_B} \times \left[\frac{1}{293} - \frac{1}{T_{amb}+273}\right]} \tag{3.19}$$

where RH_{amb} is the relative humidity in the environment of operation, RH_0 is the reference relative humidity (= 70%), T_{amb} is the ambient temperature, $E_{SD,a}$ is the activation energy, and K_B is Stefan Boltzmann's constant ($8.617 \times 10^{-5} eV$). Due to the minimal impact of RH_{amb} on the FR during the operational phase of the converter, it is negected.

Effect of mechanical stress on the SD's failure rate

Vibrations, thermal cycling, and assembly tolerances can all induce mechanical stress on a SD's bond wire, and over time, this repeated stress can lead to fatigue and eventually breakage of the wires, resulting in a permanent open circuit fault within the SD. Furthermore, in the case of IGBTs, the chip itself is a structured layer with different thermal expansion coefficients for each layer. During operation, temperature variations cause these layers to expand and contract at slightly different rates. If these stresses become excessive, cracks can initiate within the die, propagated by the continued operation and ultimately leading to device failure. Factors like poor die attach or insufficient clamping pressure during module assembly can also exacerbate the mechanical stress.

The work in [14] shows in detail how the impact of vibrational stress on SDs is best modeled using the Basquin equation.

$$\Pi_{Mech} = \left(\frac{G_{RMS}}{G_{RMS_0}}\right)^{1.5} \tag{3.20}$$

where G_{RMS} is the root mean square vibration amplitude in the environment considered[7], and G_{RMS_0} is the reference vibration amplitude (= 0.5). For the purposes of simplicity in the optimization problem formulation assumes the maximum amplitude in the model's domain of applicability (ie., $G_{RMS} = 40$).

[7]This reflects the magnitude of the vibrational stress incurred as derived from the Basquin equation.

Thermal effect on the SD and mean junction temperature estimation

Temperature plays a critical role in the failure rate and is modeled using the Arrhenius equation, where chemical reaction rates facilitate degradation mechanisms within the SD. As the junction temperature ($T_{SD,J}$) rises, the electrical resistance of the insulating gate oxide layer decreases, which allows for a greater flow of unwanted leakage current between the gate and drain terminals, in the case of an IGBT [9], [20]. Over time, this leakage current can erode the gate's ability to effectively control the IGBT[8] potentially leading to a runaway condition and catastrophic failure. Furthermore, during operation, IGBTs experience temperature fluctuations/swings ($\Delta T_{SD,J}$) due to switching losses and power dissipation. These repeated thermal cycles cause the expansion and contraction of the various materials within the IGBT package. Over time, this thermal fatigue can lead to stress fractures in the solder joints, delamination of the encapsulating materials, and even cracking of the IGBT die itself, which can permanently impair the IGBT's functionality.

The acceleration factor for estimating the impact of the thermal stress on the failure rate is given below. Where T_{Ref} is the reference temperature ($= T_{amb}$), and $T_{j-component}$ is the junction temperature of the SD. The equation is rewritten to ensure symbol conformity.

$$\begin{aligned} \Pi_{Thermal} &= e^{\frac{E_{SD,a}}{K_B} \times \left[\frac{1}{T_{Ref}+273} - \frac{1}{T_{j-component}+273} \right]} \\ &= e^{\frac{E_{SD,a}}{K_B} \times \left[\frac{1}{T_{amb}+273} - \frac{1}{T_{SD,J}+273} \right]} \end{aligned} \tag{3.21}$$

It must be noted that the domain of applicability of the FIDES approach has a maximum T_J of $125°C$. With that in mind, and making reference to Figure 3.3 as the basic electrical analog of heat transfer of in electronic component, we now define the expression for the junction temperature of a SD as below.

$$\begin{aligned} T_J &= P_A(R_{JC} + R_{CS} + R_{SA}) + T_A \\ &= P_A \cdot R_{SD,th} + T_{amb} \end{aligned} \tag{3.22}$$

and

$$P_A = P_{SD,Cond} + P_{SD,Sw} \tag{3.23}$$

[8]This thesis assumes IGBT as the main SD, and uses the two terms interchangeably.

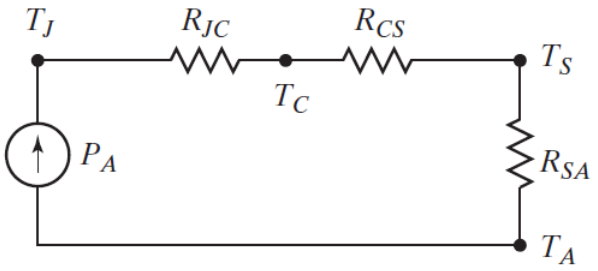


Figure 3.3: Heat transfer through an electronic component [46].

where P_A is the average power loss in a SD. R_{JC}, R_{CS}, and R_{SA} are respectively, the junction-to-case, case-to-sink, and sink-to-ambient thermal resistances lumped together as $R_{SD,th}$. $P_{SD,Cond}$ is the conduction loss, and $P_{SD,Sw}$ is the switching loss. The average conduction loss dissipated by a SD is given by the following equation.

$$P(t)_{SD,Cond} = \frac{1}{T}\int_0^T [V_{CE}(t) \cdot I_{CE}(t)]\, dt \tag{3.24}$$

Due to differences in datasheets, and the necessity to establish a common time-independent relation between all equations, it is necessary to linearize the above SD conduction loss equation, and doing so yields the following equation.

$$P_{SD,Cond} = v_{ce0} \cdot i_{SD,c} + R_{SD,On} \cdot i_{SD,c}^2 \tag{3.25}$$

where v_{ce0} is the on-state zero-current collector-emitter voltage, $i_{SD,c}$ is the collector current of the SD assuming IGBT, and $R_{SD,On}$ is the on-state resistance of the SD. The SD's switching loss is given in the (3.26) below.

$$P_{SD,Sw} = \frac{E_{sw} f_{sw}}{\pi} \cdot \frac{\sqrt{2} i_{SD,c}}{I_{rated}} \cdot \frac{\sqrt{2} V_{applied}}{V_{rated}} \tag{3.26}$$

and

$$E_{sw} = E_{sw,ref} \cdot \left(\frac{i_{SD,c}}{I_{rated}}\right)^{K_{SD,i}} \cdot \left(\frac{V_{applied}}{V_{rated}}\right)^{K_{SD,v}} \cdot [1 + TC_{sw}(T_{SD,J} - T_{amb})] \tag{3.27}$$

where E_{sw}, I_{rated}, $V_{applied}$, and V_{rated} are the total switching energy losses ($E_{sw} = E_{on} + E_{off}$), the reference/rated current[9], the operation voltage of the application, and the reference/rated blocking voltage[10] respectively. $E_{sw,ref}$ is the reference switching energy losses of the SD. $K_{SD,i}$, and $K_{SD,v}$

[9]This is assumed to be the same as the nominal maximum current under testing conditions.

[10]This is assumed to be the same as the nominal maximum voltage under testing conditions.

are the exponents that model the current and voltage dependencies on the switching energy, and TC_{sw} is the temperature coefficient of the switching losses. E_{sw} is evaluated using the analytical formula provided in [19], [54], [67], [73].

We encounter yet another challenge in (3.27) in that E_{sw} depends on $T_{SD,J}$. Here, to simplify the mathematical complexity, the maximum temperature of 125° is assumed. The values of the constants employed are tabulated in Table 3.6.

Table 3.6: Constants employed for estimating the SD's junction temperature [19], [54], [67].

Parameter	**Value**	**Parameter**	**Value**
$R_{SD,th}[°C/W]$	1.72	$R_{SD,On}[\Omega]$	0.051
$T_{amb}[°C]$	25	$I_{rated}[A]$	20
$v_{ce0}[V]$	0.82	$V_{rated}[V]$	650
K_i	0.729	K_v	1.3
TC_{sw}	0.003		

With the above equations and constants defined, we now have a foundation for estimating the mean thermal effect on the SD.

SD temperature swing and maximum junction temperature estimation

During turn-on and turn-off events, SDs experience a surge in power dissipation, which translates to a rapid rise in $T_{SD,J}$. This transient temperature spike can exacerbate the effects of thermo-mechanical stress on the SD. Additionally, the high current surges during switching can cause localized heating within the device, further accelerating degradation mechanisms. Frequent temperature swings caused by rapid on/off cycling can magnify these transient effects and contribute to a shortened lifespan. Figures 3.4 and 3.5 are the junction temperature profile of one of the IGBTs of the half-bridge converter as simulated in Simulink. FIDES approach models the thermal cycling effect via the following equation:

$$\Pi_{TCyCase} = \left(\frac{12 \cdot N_{cy}}{t_{phase}}\right) \cdot \left(\frac{\Delta T_{cycling}}{20}\right)^4 \cdot e^{\frac{E_{SD,a}}{K_B} \times \left[\frac{1}{313} - \frac{1}{T_{max-cycling}+273}\right]} \tag{3.28}$$

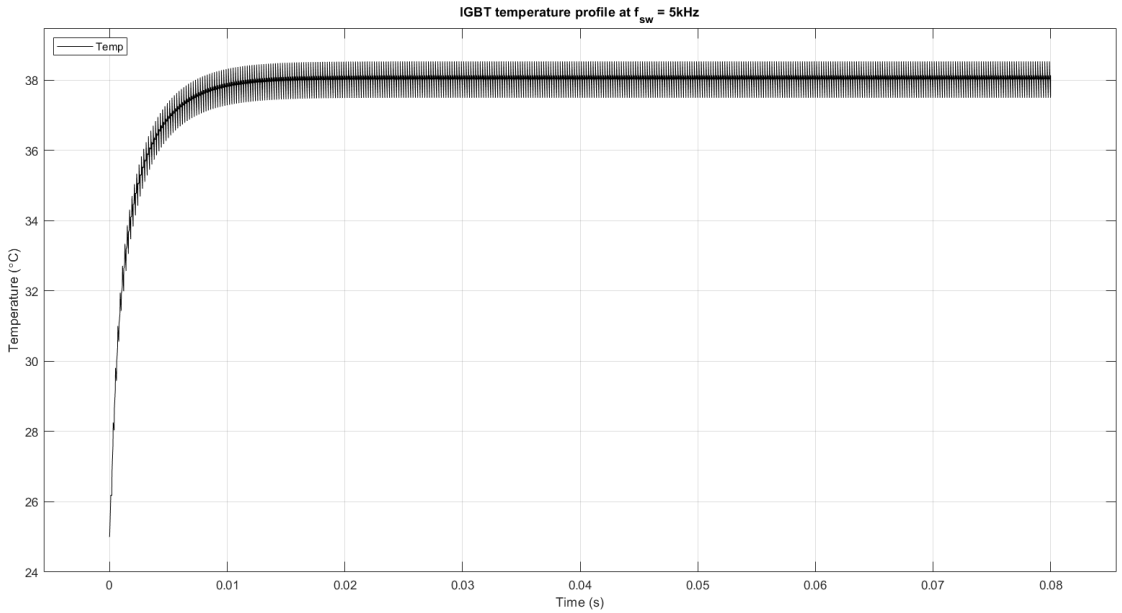


Figure 3.4: Junction temperature profile of an IGBT at $5kHz$.

where N_{cy} is the number of cycles associated with each cycling phase[11], $\Delta T_{cycling}$ is the thermal amplitude of the cycle, and $T_{max-cycling}$ is the maximum temperature reached during the cycle. It would be prudent to restate the equation using established variables to enforce variable conformity:

$$\Pi_{TCyCase} = \left(\frac{12 \cdot N_{cy}}{t_{phase}}\right) \cdot \left(\frac{\Delta T_{SD,J}}{20}\right)^4 \cdot e^{\frac{E_{SD,a}}{K_B} \cdot \left[\frac{1}{313} - \frac{1}{T_{SD,J,max}+273}\right]} \tag{3.29}$$

Intrinsically, both $\Delta T_{SD,J}$ and $T_{SD,J,max}$ depend on the value of $T_{SD,J}$ [7]. The relationships between the variables are expressed in the equations below.

$$T_{SD,J} = T_{SD,J,min} + \frac{1}{2} \cdot \Delta T_{SD,J} \tag{3.30}$$

$$T_{SD,J,min} = T_{amb} + R_{SD,th} \cdot P_{A,min} \tag{3.31}$$

$$\Delta T_{SD,J} = T_{SD,J,max} - T_{SD,J,min} \tag{3.32}$$

where $P_{A,min}$ is the minimum total power dissipated in the SD during its operation. The above equations pre-suppose that $P_{A,min}$ is known, and this might not always be the case. Due to the non-existence of a universal model to properly represent the inter-dependence, curve-fitting techniques in MATLAB were employed. By running a couple of simulations to determine the thermal relationship

[11] Assuming two cycles per day, 730 cycles per year.

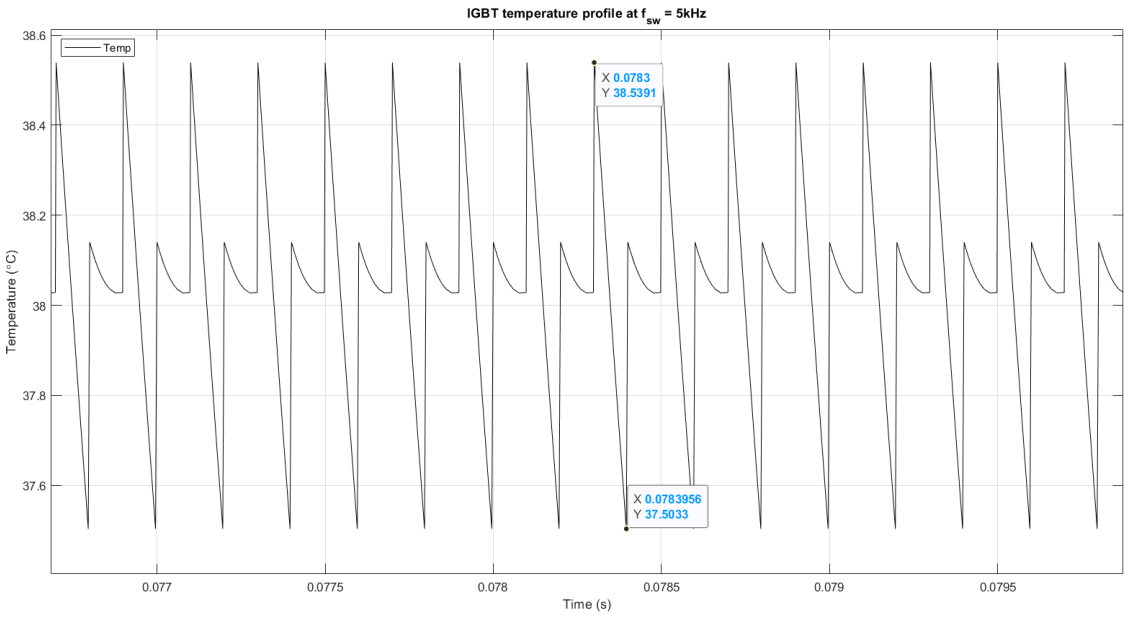


Figure 3.5: Junction temperature swing profile of an IGBT at $5kHz$.

on a half-bridge converter, the correlation among $T_{SD,J}$, $\Delta T_{SD,J}$, and $T_{SD,J,max}$ across varying f_{sw}. The correlation is given in Table 3.8 below.

Table 3.7: Correlation among the three temperature variables

$T_{SD,J}$	$\Delta T_{SD,J}$	$T_{SD,J,max}$
1	-0.1813	0.9999
-0.1813	1	-0.1781
0.9999	-0.1781	1

Whereas $T_{SD,J,max}$ has a strong positive correlation coefficient of determination ($R^s = 0.9999$) with $T_{SD,J}$, this is not the case for $\Delta T_{SD,J}$, which not only has a very low R^2 value but also a negative correlation. This makes it difficult to establish a proper model to represent $\Delta T_{SD,J}$. However, as shown in Figure 3.6, a polynomial combination of the first degree of both $T_{SD,J}$ and $T_{SD,J,max}$ yields a better model with an R^2 value of 0.8813. The second and third-order polynomial curve-fits yield even better R^2 values of 0.8864 and 0.9335, respectively, albeit at the cost of increasing the mathematical complexity of the model. For this reason, the first order model is maintained in formulating the optimization problem. The models with the determined coefficients are given in the

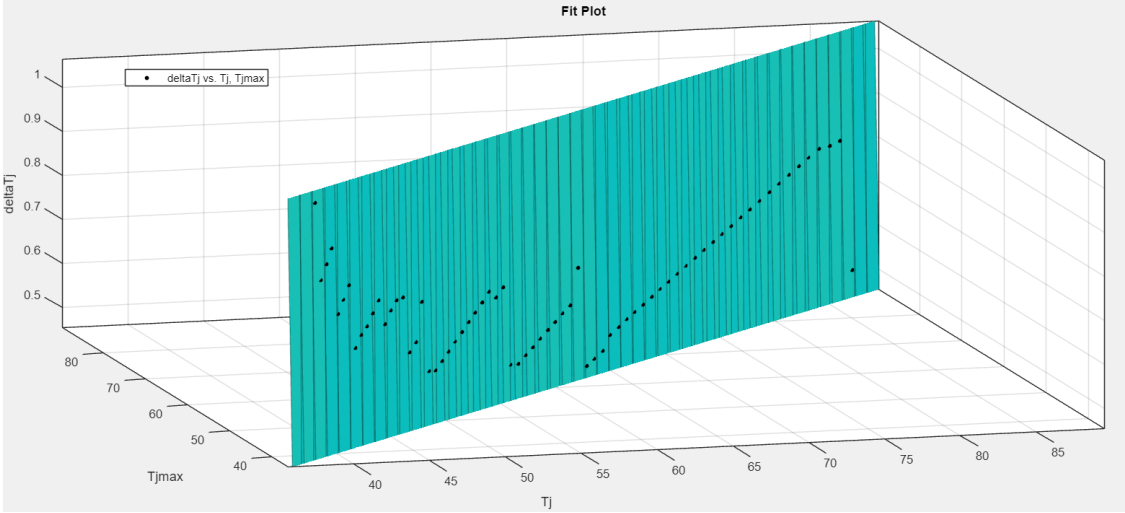


Figure 3.6: Representing $\Delta T_{SD,J}$ in terms of $T_{SD,J}$ and $T_{SD,J,max}$.

equations below.

$$T_{SD,J,max} = 0.2801 + T_{SD,J} \tag{3.33}$$

$$\Delta T_{SD,J} = 0.1977 - 2.0113 \cdot T_{SD,J} + 2.01 \cdot T_{SD,J,max} \tag{3.34}$$

To represent the CTE mismatch created in a SD during temperature swings, $\Pi_{TCySolderJoints}$ is modeled as follows [14]:

$$\Pi_{TCySolderJoints} = \left(\frac{12 \cdot N_{cy}}{t_{phase}}\right) \cdot \left(\frac{min(\theta_{cy}, 2)}{2}\right)^{\frac{1}{3}} \cdot \left(\frac{\Delta T_{SD,J}}{20}\right)^{1.9} \times e^{\frac{E_{SD,a}}{K_B} \cdot \left[\frac{1}{313} - \frac{1}{T_{SD,J,max}+273}\right]} \tag{3.35}$$

where θ_{cy}[12] is the cycle duration in hours. The fatigue coefficient of 1.9 is adopted from [14] for tin-lead solder joints, which is applicable for other types of solder joints as well. The acceleration power of the duration factor is also adopted as 1/3. From the half-bridge converter simulations conducted in Simulink, Table 3.9 and Figures 3.7 and 3.8 are shown here to indicate the magnitude of the impact of the switching losses.

Switching device reliability improvement techniques

Having established the factors that tend to impact the failure rate (FR) of the SD, we now

[12] $\theta_{cy} = t_{phase}/N_{cy}$

Table 3.8: Effect of varying switching frequency on junction temperature

$f_{sw}[kHz]$	$T_J[^\circ C]$	$\Delta T_J[^\circ C]$	$P_{SD,Cond}$	$P_{SD,Sw}$
5	38.0212	1.0358	16.4570	15.5156
10	43.2476	0.7470	15.4566	30.5427
15	48.9900	0.5756	15.9029	46.8439
20	55.1206	0.7161	15.9814	64.5941
25	61.9284	0.7100	15.8340	83.9952
30	69.4909	0.6050	15.7688	105.2886
35	77.7225	0.7240	15.6811	128.7606
40	87.0241	0.5173	15.4843	154.7585

turn our attention to the established means of minimizing this FR and thus improving its reliaibility.

Reliability improvement via passive and active means

Due to the generation of heat within power devices from on-state and switching losses, it is essential to dissipate the thermal energy that is generated from the power losses in order to maintain the operating junction temperature ($T_{SD,J}$) within specified limits or within specified temperature constraints as we shall see later in the optimization problem formulation.

Many power electronic devices are operated/designed in a way as to cut off the operation in the event of a heat dissipation failure. While various methods such as conduction, convection, radiation, or natural or forced air can facilitate this heat transfer; convection cooling is often preferred in industrial settings due to its effectiveness in managing the thermal energy produced within power devices. The literature on improving reliability by thermal management offers valuable insights into the fundamental principles, key objectives, and potential of both passive and active thermal control methods for PECs. Several sources have systematically analyzed these methods and discussed their implications [32], [41]. Additionally, the application of active thermal control methods for PEC components is highlighted in the resources to emphasize the importance of understanding and managing the thermal characteristics of PEC systems to ensure their reliability.

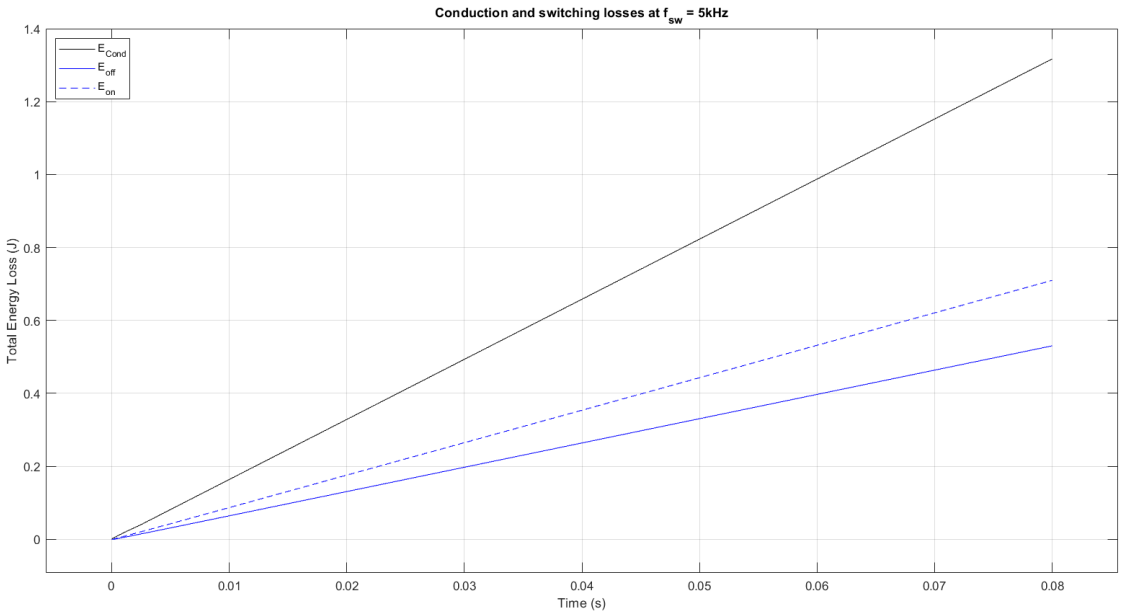


Figure 3.7: Conduction and switching energy losses in an IGBT in a half-bridge converter operating at $5kHz$.

Power electronic converters are increasingly used in high-voltage applications due to their scalability and controllability. Thermal management is crucial for reliable operation, especially in the case of MMCs, as high temperatures can lead to device degradation and failure. This is essential because traditional methods for thermal management are often reactive and cannot adapt to changing operating conditions. In [51], the authors propose a multi-objective optimization method that simultaneously minimizes the difference in thermal loading between individual MMC submodules as well as the deviation of the output current from the reference value. The optimization problem is formulated using a mixed-integer linear programming (MILP) approach. Also, a finite control set model predictive control (FCS-MPC) scheme is used to implement the optimal switching sequence. The paper first establishes a thermal model of the MMC, considering heat generation, conduction, and convection. The optimization problem is formulated with the objective functions and constraints related to thermal loading and output current control. An MILP solver is used to find the optimal switching sequence for each control cycle. The FCS-MPC scheme translates the optimal switching sequence into control signals for the MMC. This research focuses only on the switching frequency (f_{sw}) as the active thermal control method, without going into the control aspect, as much work has been done in that regard.

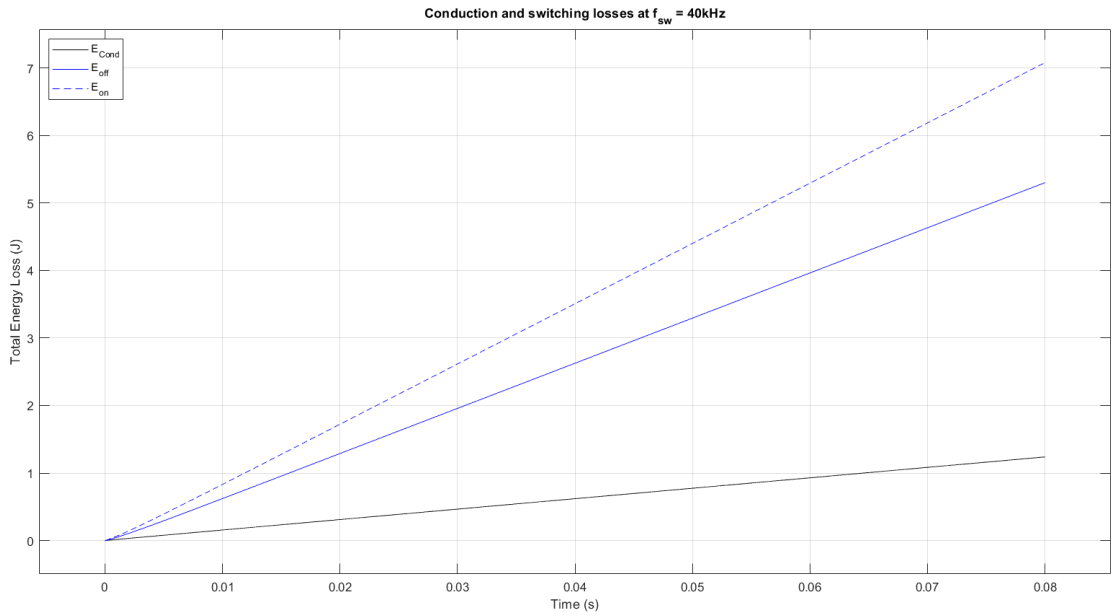


Figure 3.8: Conduction and switching energy losses in an IGBT in a half-bridge converter operating at $40kHz$.

As seen in the literature review chapter and equation (3.26), whereas higher switching frequencies allow for miniaturization, this is achieved at the expense of increased switching losses. The dissipation of heat generated during its operation is typically facilitated through the use of heatsinks, which provide a path for heat transfer from the semiconductor device (SD) to the surrounding environment. The size and design of the heatsink play a crucial role in determining the effectiveness of thermal dissipation. The proper design of heat sinks is identified as one of the passive means of dissipating generated heat from conduction and switching, as shown in Figure 3.9 [39], [49], [51].

Larger heat sink sizes provide larger surface area for free heat dissipation but at the expense of space and volume of the overall power electronic converter system. On the other hand, smaller heat sink sizes stand the risk of having higher thermal resistances and mitigating the effecting thermal dissipation from the junction temperature of the SD. Therefore, constraints on heat sink size may include maximum dimensions to fit within the available space and weight limitations to avoid overloading mounting structures. The selection of an appropriate heat sink size involves balancing the thermal dissipation requirements of the SD with practical considerations such as space limitations and manufacturability.

The design of a heat sink entails many factors, as discussed in [65], and will not be discussed

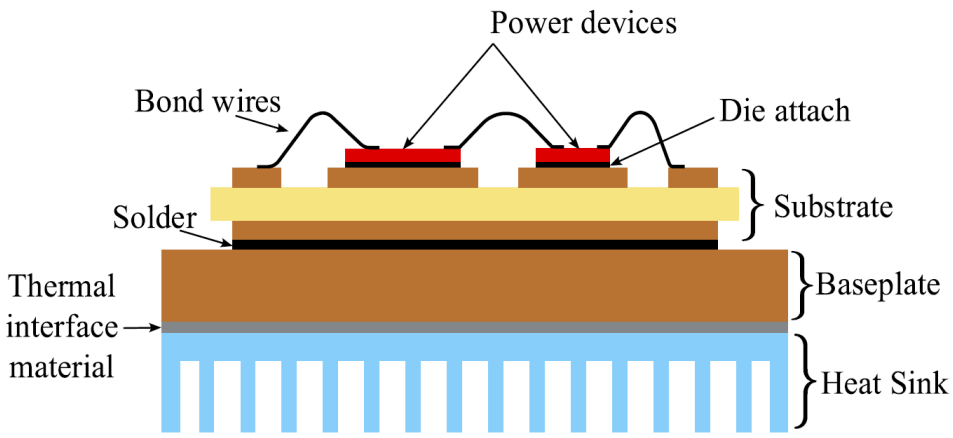


Figure 3.9: Application of a heatsink in switching device [72].

here. However, this paper identifies the base thickness ($t_{hs,b}$) as one of the design parameters[13] for the optimization. Furthermore, this paper focuses on the area of the heat sink (A_{hs}) in determining the size, as opposed to the volume of the heat sink. This is because, in the context of heat transfer, the primary purpose of a heat sink is to facilitate heat transfer from the SD to the surrounding environment. Heat transfer primarily occurs through convection, which depends on the surface area available for air to interact with the heatsink. While volume plays a role in providing mass for heat dissipation, it's ultimately the surface area that dictates the rate of heat transfer. This is because a larger volume with a poorly designed surface area might not be as effective as a smaller volume with a well-designed and maximized surface area. For these reasons, heatsink designs typically prioritize maximizing surface area within volume constraints. Fin structures, for example, increase surface area without significantly increasing volume.

As mentioned earlier this thesis does not focus on optimizing the design of the surface area of the heatsink, a general focus is made on the surface area in the optimization analysis as going in that direction presents more direct and relevant connection to heat generation and dissipation. Without considering the fin surface area[14], the area of a heat sink is given in (3.36) below.

$$A_{hs} = \frac{t_{hs,b}}{k_{hs} \times R_{hs,th}} \tag{3.36}$$

where A_{hs}, $t_{hs,b}$, and $R_{hs,th}$ are the surface area, the thickness of the base, and the thermal resistance of the heat sink, respectively. k_{hs} is the thermal conductivity of the heatsink material assuming

[13] Another term for this in optimization problem formulations is the degree of freedom.

[14] This is done for two reasons: (a) to minimize the mathematical complexity of the problem, and (b) to limit the type of design to only one cuboid shape since there can be a myriad of fin-shape designs for the heat sink.

aluminum (Al) is used. Because the heat must be conducted from the SD case to the attached heat sink, which serves as the primary cooling medium [65]. The design of the heat sink must consider the necessary thermal resistance required in order to facilitate proper heat dissipation. The relationship between the thermal resistance and the thermal power to be dissipated is given in (3.37) with reference to (3.22).

$$(R_{JC} + R_{CS} + R_{hs,th}) = \frac{T_{SD,J} - T_{amb}}{P_A} \tag{3.37}$$

The diameter size of the bond wire has also been identified as another influencing parameter on SD's FR [52]. The diameter of the bond wire ($D_{SD,bw}$) directly impacts the SD's current-carrying capability, thermal performance, manufacturability and mechanical integrity, and optimizing $D_{SD,bw}$ involves balancing these factors to prevent overstressing the wire while ensuring efficient electrical conduction and thermal dissipation. The impact of the bond wire diameter on the lifetime requires consideration since increasing the bond wire diameter not only allows the flow of a large amount of current but doing so also increases the available area for soldering, thereby improving the mechanical resilience to vibrations and thermal stress. Typically, as pointed out in [52], bond wires for IGBTs were manufactured to have very thin diameters as small as $75\mu m$ however, due to proliferation in reliability requirements and other electrical performance factors, including high energy density, modern IGBTs are assembled with bond wires in the ranges of $300\mu m - 500\mu m$.

The effect of bond wire diameter on the maximum amount of current that is allowed to flow through the bond wire is governed by the Preece equation and stated here in (3.38) for reference. The classical Preece equation did not consider the impact of the length of the bond wire on the temperature variation. In other words, the original equation is only applicable to wires in a vacuum. Furthermore, the length of the conductor tends to cause an impact on the maximum current-carrying capability of the conductor, which in turn has an impact on the thermal distribution along the conductor, although, for short pieces of conductors, it can be assumed constant [35]. This phenomenon is governed by the Joule heating effect ($Q_{gen} = I^2 \cdot R$).

$$i_{SD,c} = k_{bw} \cdot D_{SD,bw}^{3/2} \tag{3.38}$$

As previously mentioned, selecting a bond wire that is too small may lead to increased resistance, voltage drop, and power losses, potentially compromising device efficiency and reliability.

Conversely, using a $D_{SD,bw}$ that is too large can result in mechanical stresses, wire deformation (particularly during thermal cycling or mechanical shock), and reduced flexibility, leading to potential damage of detachment during operation[15]. Furthermore, SD $D_{SD,bw}$ are typically selected to be no more than 1/4 to 1/3 of the size of the bond pad on the SD chip [16]. This constraint ensures that the bond wire can be properly accommodated on the pad without exceeding the pad dimensions.

In order to establish an acceptable constraint on $D_{SD,bw}$, the classical design for wire fusing developed by W. H. Preece and modified in [35] is employed here. The modified equation factors in how the diameter and the length of the bond wire impact the current flow (current-carrying capability)of the bond wire.

$$i_{SD,c} = \frac{\pi}{4}\sqrt{\frac{k_{bw}}{\rho_{bw}}} \cdot \frac{D_{SD,bw}^2}{l_{bw}} \cdot \sqrt{\Delta T_{bw}} \tag{3.39}$$

where k_{bw} is the thermal conductivity of the bond wire, ρ_{bw} is the resistivity ($1.68 \times 10^{-8}\Omega m$ for Cu), l_{bw} is the bond wire length, and ΔT_{bw} is the temperature difference between the two ends of the bond wire (assumed constant).

Current and voltage deration are other crucial strategies to extend the lifetime of power components. To improve the SD's FR, a derating factor is applied to both $i_{SD,c}$ and $V_{applied}$, resulting in operational values that are lower than their rated values. The de-rating factor is chosen based on the desired lifetime and application requirements. Furthermore, derated $i_{SD,c}$ conversely leads to lower $T_{SD,J}$ hence lower thermal stress on the SD.

While derating offers significant benefits for the SD's lifetime and reliability, it does come with some drawbacks, including but not limited to reduced output power, increased system size, and lower efficiency at lower power levels. In reference to the first point, by limiting $i_{SD,c}$ and $v_{SD,ce}$, you inherently limit the device's ability to handle high power levels and this can be a concern for applications where maximum power output is critical. On the second point, to compensate for the reduced power capability of a derated SD, designers might have to use larger components or additional SDs in parallel to achieve the desired power output. This can lead to a larger and potentially more complex system design requiring more space and potentially higher costs for additional components. Finally, IGBTs typically exhibit higher efficiency at higher operating currents. When

[15]This phenomenon is also known as bond wire lift-off.

derated and operating at lower current levels, the switching and gate charge losses become a significant portion of the total power dissipation, and this can result in a slightly lower overall efficiency, especially at partial loads.

Considering the above factors, a common deration percentage for both $i_{SD,c}$ and $v_{SD,ce}$ is 80%[16]. The deration constraint is stated below.

$$\frac{v_{SD,ce}}{V_{rated}} = \frac{i_{SD,c}}{I_{rated}} \geq 80\% \tag{3.40}$$

Reliability improvement via parallel redundancy

As mentioned in the literature review chapter, in some safety-critical applications, achieving fault-tolerant control becomes paramount, and redundancy as a means of this approach involves incorporating multiple identical components or subsystems within the control system. This creates a level of redundancy where a single component failure doesn't cripple the entire system [33]. This is shown in Figure 3.10.

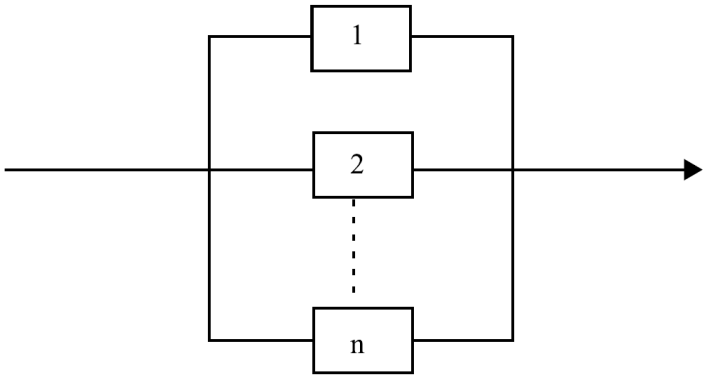


Figure 3.10: Parallel redundancy of components for FTC strategy [33].

It is important to note here that we do not consider fault detection, isolation mechanisms, and control systems as that is beyond the scope of this work. Only the reliability of the component itself is considered. It is also assumed all SDs have the same basic FRs. Once the FR of a single SD is determined using the FIDES approach, the total FR considering the optimum number of redundancy in the constraint is also determined using the approach presented in [33]. This is given

[16] $v_{SD,ce} = V_{applied}$

in (3.40) through (3.42) below.

$$R(T) = e^{-\lambda \cdot T} \tag{3.41}$$

$$R_S = 1 - [1 - R(T)]^{N_{Comp}} \tag{3.42}$$

$$\lambda_{S,Comp} = \frac{-\frac{\delta}{dt} R(T)_S}{R(T)_S} \tag{3.43}$$

$$MTTF = \int_0^\infty R(T)_S dT \tag{3.44}$$

where $\lambda_{S,Comp}$ is the system failure rate of components in parallel, $R(T)_S$ is the parallel-redundant-system reliability given mission time 'T'[17], N_{Comp} is the number of components (N_{SD} for switching devices, N_{Cap} for capacitors). $\lambda_{S,Comp}$ is the system failure rate after redundancy and MTTF is the estimated mean time to failure.

Following the discussion above on the reliability improvement methods, we are faced with the question of how much is enough. In other words, what switching frequency combined with what heat sink size or number of redundancies would yield the minimum FR and maximum MTTF given the application considered? Having defined all the factors and design parameters influencing $\lambda_{SD,useful}$, we can focus our attention on the problem formulation for the SDs failure rate that seeks to answer this question.

Genetic Algorithm Optimization Technique

The standard form for optimization problems establishes a common framework for expressing various optimization tasks. It typically applies to linear programming (LP) problems, but the core concepts can be extended to other domains. In this form, the objective function, which represents the quantity to be minimized or maximized, is a linear combination of decision variables. These variables are further constrained by a set of linear inequalities or equations. The standard form enforces non-negativity for all decision variables, simplifying the problem structure and enabling efficient solution algorithms like the Genetic Algorithm (GA). This allows for a clear separation between the objective and the feasible region defined by the constraints, facilitating the systematic search for optimal solutions within that space [40]. The standard form is stated here for reference.

[17] This is the same as t_{phase} employed earlier.

Find a vector of optimization variables, $x = (x_1, x_2, ..., x_n)^T$, in order to

Minimize an objective (or cost) function, $f(x)$

Subject to

$g_i(x) \leq 0 \qquad i = 1, 2, ..., m \qquad$ Less than type inequality constraints (LE)

$h_i(x) = 0 \qquad i = 1, 2, ..., p \qquad$ Equality constraints (EQ)

$x_{iL} \leq x_i \leq x_{iU} \qquad i = 1, 2, ..., n \qquad$ Bounds on optimization variables

The application of Genetic Algorithms (GAs) opens new avenues for optimizing the identified PEC reliability metrics, offering solutions that traditional methods may not provide. By systematically analyzing and enhancing the design and operational parameters, the optimization method aims to minimize the failure rates (λ) or, in some cases, as we will later see, maximize the lifetime and cycles to failure, thus enhancing overall system robustness. Among the various optimization approaches, GA has gained prominence due to its ability to efficiently explore complex solution spaces and find near-optimal solutions in multi-dimensional problems by following the following summarized steps:

1. Initialize a random population of potential solutions and evaluate their fitness based on the objective function.
2. Select and reproduce (crossover) the solutions with higher fitness scores.
3. Introduce random variations (mutations) to maintain selection diversity and replace the weak with new generations.
4. Continue the cycle until a predefined number of generations or stopping criterion is met, and the individuals with the highest fitness score in the final generation are considered the optimal solution.

Single objective optimization problem formulation for the SD's useful failure rate

It is important to note that cost constraints and space constraints mostly, if not always, play

a major role depending on the industry of relevance. As such, these factors are taken into consideration in the problem formulation. Furthermore, in some cases, certain manufacturability constraints must be considered. This could be the production of only certain sizes of bond wire diameter or even the heat sink base thickness. This constraint is modeled into the problem formulation as discrete variables.

Following the methodology, analysis, and all assumptions made above, the single-objective optimization problem considering only SDs is formulated as below.

$$\begin{aligned} &Minimize && \lambda_{S,SD} \\ &Subject\,to && A_{hs} \leq A_{hs,max} \\ & && T_{SD,J} \leq T_{SD,J,max} \\ & && i_{SD,c} \leq i_{SD,c,rated} \\ & && \frac{V_{applied}}{V_{rated}}, \frac{i_{SD,c}}{I_{rated}} \geq 80\% \\ & && N_{SD} \leq N_{SD,max} \\ & && Space_{pcd} \leq Space_{pcb,max} \\ & && Cost_{Comp} \leq Budget_{SD} \end{aligned} \tag{3.45}$$

where $\lambda_{S,SD} = f(f_{sw}, i_{SD,c}, V_{applied}, t_{hs,b}, D_{SD,bw}, N_{SD})$. Table 3.9 shows the range of design parameters and the type of data sweep employed. Furthermore, the parameter ranges are chosen based on the "SEMIKRON SK20GD07E3ETE1" IGBT component.

Table 3.9: SD failure rate optimization design space

Parameter	**Description**	**Data Range** [Min...Max]	**Data Sweep Type**
$f_{sw}\,(kHz)$	Switching frequency	[5 ... 40]	Continuous
$i_{SD,c}\,(A)$	Collector current	[10 ... 20]	Continuous
$V_{applied}\,(V)$	Blocking voltage	[500 ... 650]	Continuous
$t_{hs,b}\,(mm)$	Heat sink base thickness	[25 ... 50]	Discrete
$D_{SD,bw}\,(\mu m)$	Bond wire diameter	[300 ... 500]	Discrete
N_{SD}	Number of SDs	[2 ... 10]	Discrete

Modeling the useful failure rate of the Cap

As we did for the SD, we employ the FIDES approach here to estimate the useful FR of the capacitor (Cap). It is stated below in (3.46):

$$\lambda_{Cap} = \lambda_{Cap,Phy} \times \Pi_{Cap,PM} \times \Pi_{Cap,Process} \tag{3.46}$$

The process factor constants employed for SDs are applicable for Caps as well. The only difference is that the basic failure rates of the two components are not the same. We assume the basic failure rate of a solid aluminum electrolytic capacitor (λ_{0Cap}).

Physical stress factors impacting the Cap's failure rate

In the case of the Cap - and also considering only the operation and maintenance phase - the FR due to physical stress contribution is given as:

$$\lambda_{Cap,Phy} = \lambda_{0Cap} \cdot \left(\frac{t_{phase}}{T_{annual}}\right)(\Pi_{ThEl} + \Pi_{TCy} + \Pi_{Mech,Cap})(\Pi_{Induced}) \tag{3.47}$$

where λ_{0Cap} is the basic failure rate of the Cap, Π_{ThEl}, Π_{TCy}, and $\Pi_{Mech,Cap}$ are the AFs that impact the Cap's FR and are described as follows. Similar to the SD, the capacitor's physical stresses are also influenced by three categories of factors according to the FIDES approach, which is presented here in Table 3.10 for reference.

Table 3.10: The capacitor's physical stress factors experienced during its operation.

AF	**Category**	**Description**
Π_{ThEl}	Thermo-Electrical	AF due to thermal and electrical influence on the capacitor
Π_{TCy}	Thermal Cycling	AF due to thermal cycling influence on the capacitor
$\Pi_{Mech,Cap}$	Mechanical	AF due to mechanical influence on the capacitor

The induced/overstress factors as discussed for the SDs are applicable for capacitors as well, the only difference is the magnitude of impact considering all other parameters constant for any given parameter. Moreover, the discussions made about the process factors on the SD are applicable to the Cap. The only process factor that is not applicatble is the Π_{PW} AF.

Effect of mechanical stress on the Cap's failure rate

Similar to the effect on SDs, vibrations can also contribute to the degradation and eventual failure of power capacitors, potentially impacting their useful failure rate. Constant vibrations can cause mechanical stress on the capacitor's internal components, similar to thermal cycling. This stress can lead to micro-fractures in the dielectric film, fatigue of electrical connections, and potential loosening of internal components. Over time, these effects can weaken the capacitor's structure and compromise its electrical performance.

The severity of the vibrational effect depends on several factors. The higher the vibrational frequency and the larger the amplitude, the greater the stress and strain on the capacitor's internal structure. Furthermore, the way the capacitor is mounted and secured within the system can significantly influence how vibrations are transmitted and the resulting stress experienced by the components. The AF that models the mechanical stress on the capacitor is given below.

$$\Pi_{Mech,Cap} = \gamma_{Mech} \cdot \left(\frac{G_{RMS}}{G_{RMS_0}} \right)^{1.5} \tag{3.48}$$

where γ_{Mech} is the mechanical acceleration factor coefficient, and G_{RMS} is the amplitude of the mechanical vibration assumed to be the same value as discussed in the case of SD.

Thermal effect on the Cap and its core temperature estimation

The combined effect of the thermal and electrical processes that accelerate the Cap's aging process and increase its FR is also modeled after the PoF and given in equation 3.49 below.

$$\Pi_{Thermo-electrical} = \gamma_{TH-EL} \cdot \left(\frac{1}{S_{ref}} \times \frac{V_{applied}}{V_{rated}} \right)^3 \cdot e^{\frac{E_{Cap,a}}{K_B} \cdot \left[\frac{1}{293} - \frac{1}{T_{amb}+273} \right]} \tag{3.49}$$

Here, γ_{TH-EL} is the thermo-electrical acceleration factor coefficient, S_{ref} is the reference level of the electrical stress on the electrolytic capacitor, $V_{applied}$ is the applied voltage in the operation, V_{rated} is the rated voltage of the capacitor, $E_{Cap,a}$ is the activation energy of the capacitor.

Cap temperature swing and maximum core temperature estimation

The repeated process of heating and cooling can significantly impact the useful failure rate of power capacitors, and this effect arises from the inherent mismatch in thermal expansion coefficients between the various materials used within the capacitor. The immediate effect of thermal-cycling is the mechanical stress at the interfaces between materials, like the dielectric film and electrodes. Over time, this repeated stress can lead to fatigue, cracking, and delamination within the capacitor, ultimately compromising its performance and potentially causing electrical breakdown. The thermal cycling AF for a power Cap is modeled as follows.

$$\Pi_{TCy} = \gamma_{TCy} \cdot \left(\frac{12 \times N_{cy}}{t_{phase}}\right) \cdot \left(\frac{min(\theta_{cy}, 2)}{2}\right)^{\frac{1}{3}} \cdot \left(\frac{\Delta T_{Cap,cycling}}{20}\right)^{1.9} \cdot e^{\frac{E_{Cap,a}}{K_B} \cdot \left[\frac{1}{313} - \frac{1}{T_{Cap,max-cycling}+273}\right]} \tag{3.50}$$

where γ_{TCy} is the thermal cycling acceleration factor coefficient, θ_{cy} cycles duration (hours), $\Delta T_{Cap,cycling}$ is the temperature rise of the capacitor, and $T_{Cap,max-cycling}$ is the maximum temperature on the board during a cycling phase ($^{\circ}C$). $\Delta T_{Cap,cycling}$ is dependent on the percent ripple current in the application relative to the output current, the equivalent series resistance (ESR) of the Cap, and the Cap's thermal resistance ($R_{Cap,th}$). Derivation of $\Delta T_{Cap,cycling}$ and $T_{Cap,max-cycling}$ are as follows [1], [17].

$$\Delta T_{Cap,cycling} = I_{rip}^2 \times ESR \times R_{Cap,th} \tag{3.51}$$

Where I_{rip} is the percent ripple current in the application relative to the rated current, ESR is the equivalent series resistance of the capacitor, and $R_{Cap,th}$ is the capacitor's thermal resistance. The percent ripple current is calculated as shown in (3.52)

$$I_{rip} = \frac{DuCy}{2R_o C f_{sw}} \tag{3.52}$$

Where $DuCy$ is the duty cycle of the application. The equivalent series resistance (ESR) represents the internal resistance of the electrolytic capacitor, including the resistance of the electrolyte and the electrodes. It provides a direct mathematical relationship to the thermal effect on the electrolytic capacitor during operation when a ripple voltage superimposes a d.c. offset voltage. The equation for the ESR is given in (3.53).

$$ESR = R_o + R_d(f) + R_e(T) \tag{3.53}$$

where R_o, R_d, R_e are the approximate constant ohmic resistance of the foil, connecting tabs, and solder terminals, the frequency-dependent resistance of the dielectric layer, and the temperature-dependent resistance of the electrolyte solution in combination with the spacer paper. This paper assumes an $R_o = 10^{-3}\Omega$ which is a typical value of the constant resistance. R_d and R_e are given below in the following equations.

$$R_d(f) = \frac{D_{ox}}{2\pi f_{sw} C} \tag{3.54}$$

$$R_e(T) = R_e(25°C) \cdot 2^{-\left[\frac{T_{Cap,c} - T_{amb}}{40}\right]^{0.6}} \tag{3.55}$$

D_{ox}, C, $R_e(25°C)$, and $T_{Cap,c}$ are the dissipation factor of the dielectric layer; the capacitance of the electrolytic capacitor; the temperature-dependent resistance at room temperature which is assumed to $0.5\,\Omega$ [17]; and the core temperature of the electrolytic capacitor. Due to unavailability of a proper mathematical model to represent $T_{Cap,c}$, we assume maximum domain applicability of the model[18].

The thermal resistance of the electrolytic capacitor ($R_{Cap,th}$) determines the Cap's ability to dissipate heat generated during its operation. It is represented in the following equation.

$$R_{Cap,th} = \frac{1}{h_{tot} \cdot A_{Cap}} \tag{3.56}$$

where

$$A_{Cap} = \frac{\pi}{4} \times D_{Cap} \times (D_{Cap} + 4 \cdot L_{Cap}) \tag{3.57}$$

$$h_{tot} = h_{free} + h_{rad} \tag{3.58}$$

$$h_{rad} = \varepsilon\sigma(T_{Cap,c} + T_{amb})(T_{Cap,c}^2 + T_{amb}^2) \tag{3.59}$$

$$h_{free} = 1.32 \times \left[\frac{T_{Cap,c} - T_{amb}}{D_{Cap}}\right]^{\frac{1}{4}} \tag{3.60}$$

In the above equations, h_{tot} is the total heat transfer coefficient, A_{Cap} is the surface area of the electrolytic capacitor (assuming a cylindrical structure), h_{free} is the heat transfer coefficient by convection, h_{rad} is the heat transfer coefficient by radiation, ε is the radiation coefficient/emissivity,

[18] $125°C$

σ is Stefan-Boltzmann's constant[19], and D_{Cap}, L_{Cap} are the diameter and length of the electrolytic capacitor respectively. We now derive the formula for $T_{Cap,max-cycling}$ in (3.61).

$$T_{Cap,max-cycling} = T_{Cap,c} + \frac{1}{2} \cdot \Delta T_{Cap,cycling} \tag{3.61}$$

Single-objective optimization problem formulation for the Cap's constant failure rate

Another constraint that is set on the capacitor's physical size to account for spacing and manufacturing is the apect ratio (AR)[20]. With the above equations defined, we can now formulate the capacitor's useful failure rate improvement optimization problem as follows.

$$\begin{aligned}
&Minimize && \lambda_{S,Cap} \\
&Subject\ to && A_{Cap} \leq A_{Cap,max} \\
& && AR_{Cap,min} \leq AR_{Cap} \leq AR_{Cap,max} \\
& && I_{rip} \leq I_{rip,max} \\
& && \frac{V_{applied}}{V_{rated}} \geq 80\% \\
& && T_{Cap,c} \leq T_{Cap,c,max} \\
& && N_{Cap} \leq N_{Cap,max} \\
& && Space_{pcd} \leq Space_{pcb,max} \\
& && Cost_{Comp} \leq Budget_{Cap}
\end{aligned} \tag{3.62}$$

where $\lambda_{S,Cap} = f(f_{sw}, V_{applied}, L_{Cap}, D_{Cap}, N_{Cap})$. N_{Cap} denotes the number of capacitors, $Space_{pcb}$ is available space on the PCB, and $Cost_{Comp}$ is the cost of total number of capacitors. As we did for the SD, Table 3.11 is shown to establish the range of design parameters and the type of data sweep employed.

Estimation of the wear-out failure rates

With reference to (3.4), the wear-out phase of the PEC's critical components is modeled using established equations, as mentioned earlier. Whereas the FIDES approach provides a means

[19]Note that the Boltzmann constant being used here is $5.67 \times 10^{-8} W/m^2K^4$, as opposed to the eV.

[20]$AR = L_{Cap}/D_{Cap}$

Table 3.11: Cap failure rate optimization design space.

Parameter	**Description**	**Data Range** [Min...Max]	**Data Sweep Type**
$f_{sw}\,(kHz)$	Switching frequency	[5 ... 40]	Continuous
$V_{applied}\,(V)$	Blocking voltage	[500 ... 650]	Continuous
$L_{Cap}\,(mm)$	Length of Cap	[7.5 ... 175]	Discrete
$D_{Cap}\,(mm)$	Diameter of Cap	[5 ... 100]	Discrete
N_{Cap}	Number of Caps	[2 ... 10]	Discrete

for estimating the random failures - which is assumed to follow a normal distribution, it is not adopted for estimating the wear-out phases of the SD and the Cap. For this reason, this research adopts different models which are discussed in this section.

Modeling the wear-out failure rate of the SD

The wear-out failure rate of a SD is best modeled as the cycles to failure [59]. The cycles to failure model for the SD is adapted from the work done in [52], which is modified and developed from the Coffin-Manson-Arrhenius model. It is adopted because the Coffin-Manson-Arrhenius model only considers the junction temperature swing and not the other influencing factors. The model is given in equation (3.63) below.

$$N_{f,SD} = K \times \Delta T_{SD,J}^{\beta_1} \times e^{\left(\frac{\beta_2}{T_{SD,J}+273}\right)} \times t_{on}^{\beta_3} \times i_{SD,c}^{\beta_4} \times v_{SD,ce}^{\beta_5} \times D_{SD,bw}^{\beta_6} \tag{3.63}$$

where K is the adopted lifetime constant, β is a vector of confidence level adopted from [52], t_{on} is the rise time of the temperature cycle, and $D_{SD,bw}$ is the diameter of the SD's bond wire. $v_{SD,ce}$ is the same as $V_{applied}$.

Single-objective optimization problem formulation for the SD's wear-out failure rate

Assuming t_{on} equal t_{phase}, and following the above established paramenters, we can now formulate the optimization problem as shown in (3.64). Furthermore, the same constraints enforced

in the FR minimization problem formulation are applied here.

$$\begin{aligned} Maximize \quad & N_{f,SD} \\ Subject\ to \quad & A_{hs} \leq A_{hs,max} \\ & T_{SD,J} \leq T_{SD,J,max} \\ & i_{SD,c} \leq i_{SD,c,rated} \\ & \frac{v_{applied}}{V_{rated}}, \frac{i_{SD,c}}{I_{rated}} \geq 80\% \end{aligned} \tag{3.64}$$

where $N_{f,SD}$ is the cycles to failure of the SD. $N_{f,SD} = f(f_{sw}, i_{SD,c}, V_{applied}, t_{hs,b}, D_{SD,bw})$, and the design parameters defined in Table 3.10 are also applicable here. One key difference here to note is that whereas the optimization problem in the case of the FR was a minimization one, it becomes one of maximization in this case. Furthermore, due to the gap in knowledge, it is very difficult to establish a lifetime model to represent more than one SD as a parallel system. For that matter, this thesis maintains a single-component reliability improvement of the wear-out phases of both the SD and Cap.

Modeling the wear-out failure rate of the Cap

The lifetime of a single electrolytic capacitor is established in [1] and [17], and emloyed here. The model takes acount of the basic lifetime of the capacitor when operated at nominal conditions, the thermal effect on the Cap's lifetime, ripple current effect, and also the impact of the operating voltage. This lifetime is stated below.

$$L_{x,Cap} = L_0 \times 2^{\frac{T_{Cap,c} - T_{amb}}{10K}} \times K_{Cap,i}^{\left[1 - I_{rip}^2\right] \cdot \frac{\Delta T_{Cap,cycling}}{10K}} \times \left(\frac{V_{applied}}{V_{rated}}\right)^{-K_{Cap,v}} \tag{3.65}$$

where $K_{Cap,i}$ is the capacitor's empirical safety factor[21]. Here, the nominal lifetime (L_0) can be obtained from the manufacturer's datasheet, which serves as the base standard for determining whether the electrolytic capacitor is going to outlive or perhaps deteriorate before its estimated nominal lifetime. Furthermore, the model incorporates a temperature factor that determines how temperature impacts the lifetime of the electrolytic capacitor. This follows Arrhenius' $10°C$ rule

[21] We assume $K_{Cap,i} = 4$, and $K_{Cap,v} = 5$ for simplicity.

which suggests that for every 10 units of temperature increase, the lifespan of an electronic component is halved. It should be noted that this is not a universally proven law but rather a general observation based on empirical data and degradation mechanisms within components, as the actual impact of temperature on the lifespan can vary significantly depending on the specific component, its materials, and operating conditions.

The model also accounts for the ripple current effect on the lifetime of the electrolytic capacitor through self-heating. Here, the ripple current rating of an electrolytic capacitor specifies the maximum RMS current the capacitor can handle at specific frequency without exceeding its temperature limitations. This is shown in [17] as the temperature of an electrolytic capacitor rises with increasing ripple current, which in turn affects the lifetime.

It is also expressed in the model how the lifetime of the electrolytic capacitor is inversely proportional to the applied voltage stress [57]. This means that operating an electrolytic capacitor at a lower than its rated voltage presents the potential to extend its lifespan hence the purpose of setting the deration constraint.

Single-objective optimization problem formulation of the Cap's wear-out failure rate

The resulting single-objective optimization problem for a capacitor is formulated as follows.

$$\begin{aligned} Maximize \quad & L_{x,Cap} \\ Subject\ to \quad & A_{Cap} \leq A_{Cap,max} \\ & AR_{Cap,min} \leq AR_{Cap} \leq AR_{Cap,max} \\ & I_{rip} \leq I_{rip,max} \\ & \frac{V_{applied}}{V_{rated}} \geq 80\% \\ & T_{Cap,c} \leq T_{Cap,c,max} \end{aligned} \tag{3.66}$$

where $L_{x,Cap} = f(f_{sw}, V_{applied}, L_{Cap}, D_{Cap})$. Similar to the case in SD, no model exists that properly represents the total lifetime of a parallel system of Caps. The design variables discussed in the Cap failure rate section in Table 3.12 are applicable to this problem form formulation.

Multi-objective optimization problem formulation of the components' useful failure rates

Now that we have established the individual optimization problem formulations, we extrapolate the models discussed thus far in order to formulate the total failure rate of the half-bridge converter containing both Caps and SDs. Making reference back to (3.3), the multi-objective optimization problem is formulated as follows.

$$
\begin{aligned}
&Minimize && \lambda_{S,SD} \\
&Minimize && \lambda_{S,Cap} \\
&Subject\ to && A_{hs} \leq A_{hs,max} \\
& && A_{Cap} \leq A_{Cap,max} \\
& && AR_{Cap,min} \leq AR_{Cap} \leq AR_{Cap,max} \\
& && T_{SD,J} \leq T_{SD,J,max} \\
& && T_{Cap,c} \leq T_{Cap,c,max} 1 \\
& && i_{SD,c} \leq i_{SD,c,rated} \\
& && \frac{V_{applied}}{V_{rated}}, \frac{i_{SD,c}}{I_{rated}} \geq 80\% \\
& && I_{rip} \leq I_{rip,max} \\
& && N_{SD} \leq N_{SD,max} \\
& && N_{Cap} \leq N_{Cap,max} \\
& && Space_{pcd} \leq Space_{pcb,max} \\
& && Cost_{SD,\,Cap} \leq Budget_{SD,\,Cap}
\end{aligned}
\tag{3.67}
$$

where $(\lambda_{S,SD}\ \&\ \lambda_{S,Cap}) = f\,(f_{sw}, V_{applied}, i_{SD,c}, t_{hs,b}, L_{Cap}, D_{Cap}, D_{SD,bw}, N_{SD}, N_{Cap})$. The minimization problem here is to find the vector of control parameters that yield the minimum failure rate of both the switching device and the capacitor.

Multi-objective optimization problem formulation of the components' wear-out failure rates (lifetimes)

As done for the failure rates, we formulate the total wear-out failure rate of the converter, making reference to (3.4) and considering both the cycles to failure and the lifetime of the capacitor.

$$
\begin{aligned}
Maximize \quad & N_{f,SD} \\
Maximize \quad & L_{x,Cap} \\
Subject\ to \quad & A_{hs} \leq A_{hs,max} \\
& A_{Cap} \leq A_{Cap,max} \\
& AR_{Cap,min} \leq AR_{Cap} \leq AR_{Cap,max}1 \\
& T_{SD,J} \leq T_{SD,J,max} \\
& T_{Cap,c} \leq T_{Cap,c,max} \\
& i_{SD,c} \leq i_{SD,c,rated} \\
& \frac{V_{applied}}{V_{rated}}, \frac{i_{SD,c}}{I_{rated}} \geq 80\% \\
& I_{rip} \leq I_{rip,max} \\
& Space_{pcd} \leq Space_{pcb,max} \\
& Cost_{SD,\,Cap} \leq Budget_{SD,\,Cap}
\end{aligned}
\tag{3.68}
$$

where $(N_{f,SD}\ \&\ L_{x,Cap}) = f\left(f_{sw}, V_{applied}, i_{SD,c}, t_{hs,b}, L_{Cap}, D_{Cap}, D_{SD,bw}\right)$. The goal here, is to find the set of optimum parameters that yield the maximum switching device cycles to failure as well as capacitor lifetime.

CHAPTER 4

RESULTS AND ANALYSIS

This chapter presents the results and analysis of the research conducted to optimize the reliability of a half-bridge converter using Genetic Algorithm (GA). The primary objective was to identify the influencing parameters that impacted the failure rates (FR) or lifetimes of the most critical components (SDs and Caps) and characterize them as control/design parameters for optimization that would lead to a significant improvement in the converter's Mean Time To Failure (MTTF) - hence its reliability - while maintaining acceptable design constraints. Specifically, this study aimed to:

1. Identify key parameters that influence converter reliability.
2. Adopt and develop a Genetic Algorithm-based optimization model.
3. Evaluate the improvement in reliability through comprehensive testing and analysis.

In other words, this research tests the following two hypotheses: the application of GA can identify optimal parameter sets that significantly improve converter reliability, and optimized half-bridge converters will demonstrate a higher MTTF compared to non-optimized counterparts.

Genetic Algorithm (GA) optimization options employed

The first step was to identify appropriate reliability models that holistically represented the converter's FR and lifetime. For the FR, the most current model was considered to be the FIDES approach, which incorporates the components physics of failure (PoF) along with all major reliability influencers including but not limited to temperature, mechanical vibrations, and electrical overstress factors. Furthermore, in the case of the lifetimes, the models were adapted from the works of [1] and [52] which also gives a more current representation of the remaining lifetime and cycles to failure. The four adopted fitness functions are restated here for reference:

$$\lambda_{SD} = \lambda_{SD,Phy} \times \Pi_{SD,PW} \times \Pi_{SD,PM} \times \Pi_{SD,Process} \tag{4.1}$$

$$\lambda_{Cap} = \lambda_{Cap,Phy} \times \Pi_{Cap,PM} \times \Pi_{Cap,Process} \tag{4.2}$$

$$N_f = K \times \Delta T_{SD,J}^{\beta_1} \times e^{\left(\frac{\beta_2}{T_{SD,J}+273}\right)} \times t_{on}^{\beta_3} \times i_{SD,c}^{\beta_4} \times v_{SD,ce}^{\beta_5} \times D_{SD,bw}^{\beta_6} \tag{4.3}$$

$$L_{x,Cap} = L_0 \times 2^{\frac{T_{Cap,c}-T_{amb}}{10K}} \times K_i^{\left[1-I_r^2 ip\right]\cdot\frac{\Delta T_{Cap,cycling}}{10K}} \times \left(\frac{V_{applied}}{V_{rated}}\right)^{-K_{Cap,v}} \tag{4.4}$$

where (4.1) and (4.2) model the useful FRs (random-phase) of switching devices (SDs) and capacitors (Caps) respectively. (4.3) and (4.4) on the other hand represent the cycles to failure or lifetime (wear-out phase). This is properly shown in Table 4.1 below.

Table 4.1: Fitness functions employed and the phases they represent.

Objective	**Fitness Function**	**Description**	**Failure phase**
Minimize	λ_{SD}	Switching device failure rate	Random failure
Minimize	λ_{Cap}	Capacitor failure rate	Random failure
Maximize	$N_{f,SD}$	Switching device cycles to failure	Wear-out
Maximize	$L_{x,Cap}$	Capacitor remaining lifetime	Wear-out

Following the analysis of the models, the various parameters were selected as the design parameters that offered some degree of freedom of control. Table 4.2 identifies all the chosen parameters. The fitness functions that they influence are also indicated appropriately.

Regarding the GA optimization parameters, Table 4.3 shows the choice of optimization details as adopted from the MATLAB documentation, depending on the number of optimization parameters or whether a single or multiobjective optimization problem is considered. Where $nVars$ represents the number of optimization variables, SOOP represents a single-objective optimization problem, and MOOP is a multi-objective optimization problem.

Furthermore, various empirical constants were adopted from multiple works and employed in this study. These are tabulated in Table 4.4 below. The left hand of the table indicates the constants used for the SD's estimations, while the right hand indicates the constants used in the Cap's estimations. More details can be found in the respective studies [1], [14], [17], [52].

Table 4.2: Design parameters and their fitness functions.

Parameter	**Description**	**Dependent fitness function**
$V_{applied}$	Application voltage	λ_{SD}, λ_{Cap}, $N_{f,SD}$, L_{Cap}
f_{sw}	Switching frequency	λ_{SD}, λ_{Cap}, $N_{f,SD}$, L_{Cap}
$i_{SD,c}$	Collector current	λ_{SD}, $N_{f,SD}$
L_{Cap}	Capacitor length	λ_{Cap}, L_{Cap}
D_{Cap}	Capacitor diameter	λ_{Cap}, L_{Cap}
$t_{hs,b}$	Heat sink base thickness	λ_{SD}, $N_{f,SD}$
$D_{SD,bw}$	bond wire diameter	λ_{SD}, $N_{f,SD}$
N_{SD}	Number of SDs	λ_{SD}, λ_{Cap}, $N_{f,SD}$, L_{Cap}
N_{Cap}	Number of Caps	λ_{SD}, λ_{Cap}, $N_{f,SD}$, L_{Cap}

Table 4.3: Details of the GA parameters employed.

Parameter	**Value**
Population size	50 when $nVars \leq 5$, 200 otherwise
Maximum generations	$100 \times nVars$ for SOOP, $200 \times nVars$ for MOOP
Elite count	ceil($0.05 \times$ Population Size)
Function tolerance	e^{-6} for SOOP, e^{-4} for MOOP

Single-objective optimization of the SD's useful failure rate ($\lambda_{SD,useful}$)

Depending on the maximum and minimum constraints set on the SD's failure rate model (3.45), the GA optimization searches the design space for the minimum solution accordingly. The optimum design parameters returned for the SD SOOP are tabulated as shown in Table 4.5. It must be noted that the results, depend very much on the constraints set on the fitness functions[1].

Following the GA optimization, the algorithm converges after 53 generations with a mean penalty of 0.0092. An observation of Table 4.5 shows key insights into the operation of the converter. First, it can be noted from the upper half of the table that a single SD, when optimized based on the given

[1]This applies not only to this case, but to all the optimization cases in this research.

Table 4.4: Empirical constants employed for the FR and lifetime estimations.

SD		**Cap**	
Constant	**Value**	**Constant**	**Value**
$Part\_Grade$	1	✓	✓
$Recom\_Grade$	1	✓	✓
$Process\_Grade$	1	✓	✓
$E_{sw,ref}$	0.625×10^{-3}	γ_{Th-El}	0.69
$T_{amb}\,[^{\circ}C]$	25	✓	✓
$v_{ce0}\,[V]$	0.82	γ_{TCy}	0.26
$I_{rated}\,[A]$	20	γ_{Mech}	0.05
$V_{rated}\,[V]$	650	✓	✓
$R_{SD,on}\,[\Omega]$	0.051	ε	0.85
$R_{SD,th}\,[W/^{\circ}C]$	1.72	$\sigma\,[W/m^2K^4]$	5.67×10^{-8}
$K_{SD,v}$	1.3	D_{ox}	0.015
$K_{SD,i}$	0.729	$C\,[mF]$	7.312
K	2.4×10^{4}	$R_e(25^{\circ}C)\,[\Omega]$	0.5
TC_{sw}	0.003	$R_o\,[\Omega]$	0.01
$E_a\,[eV]$	0.122	$E_a\,[eV]$	0.1
K_b	8.617×10^{-5}	✓	✓
G_{RMS_0}	0.5	✓	✓
$K_{hs}\,[W/m \cdot^{\circ} C]$	160	$L_0\,[yr]$	1
$K_{bw}\,[W/m \cdot^{\circ} C]$	390	$DuCy$	0.585
$\rho_{bw}\,[\Omega m]$	1.68×10^{-8}	$K_{Cap,i}$	4
$l_{bw}\,[m]$	1.7×10^{-3}	$K_{Cap,v}$	5
$\Delta T_{bw}\,[^{\circ}C]$	1.1	–	–

constraints, yields the above optimum operating parameters as well as a FR of 658.18×10^{-5} FIT, which is fairly good when compared to its base failure rate ($\lambda_{0TH} = 0.56$). The optimum returned failure rate solution corresponds to a MTTF of 151.93 $[hrs]$. As stated earlier, this result is tied to the stipulated design constraints.

Table 4.5: Switching device failure rate optimization design results.

$\boldsymbol{\Delta}$	**Design parameter**	**Optimum Value**	**Constraint**	**Min/Max Value**
$1\ SD$	$f_{sw}\ (kHz)$	5.002	$T_{J,max}\ [°C]$	≤ 125
	$i_{SD,c}\ (A)$	15.98	$Der\ [\%]$	≥ 80
	$V_{applied}\ (V)$	519.35	$A_{hs,max}\ [mm^2]$	$\leq 5000 \times 10^{-6}$
	$t_{hs,b}\ (mm)$	30	$i_{SD,c,max}\ [A]$	≤ 20
	$D_{SD,bw}\ (\mu m)$	400	–	–
	$\boldsymbol{\lambda_{0TH}}\ [FIT]$		0.56	
	$\boldsymbol{\lambda_{SD}}\ [FIT]$		658.18×10^{-5}	
	$\boldsymbol{R_S}(T)\ [\%]$		93.63	
	$\boldsymbol{MTTF}\ [hrs]$		151.9341	
$\geq 2\ SDs$	$f_{sw}\ (kHz)$	5.001	$T_{J,max}\ [°C]$	≤ 125
	$i_{SD,c}\ (A)$	15.98	$Der\ [\%]$	≥ 80
	$V_{applied}\ (V)$	519.24	$A_{hs,max}\ [mm^2]$	$\leq 5000 \times 10^{-6}$
	$t_{hs,b}\ (mm)$	45	$i_{SD,c,max}\ [A]$	≤ 20
	$D_{SD,bw}\ (\mu m)$	500	$Space_{pcb}\ [\#]$	≤ 20
	N_{SD}	8	$Budget_{SD}\ [\$]$	≤ 500
	$\boldsymbol{\lambda_{S,SD}}\ [FIT]$		639.46×10^{-10}	
	$\boldsymbol{R_S}(T)\ [\%]$		100	
	$\boldsymbol{MTTF}\ [hrs]$		412.9352	

Observing the lower half of Table 4.5 shows that an even better result can be achieved when fault-tolerance via redundancy is incorporated into the optimization. In other words, assuming a design engineer has the option of incorporating a maximum of 20 SDs - that is, 9 redundant SDs for each of the two main SDs in the case of a half-bridge converter - based on the constraints, the optimum selection would be 8, that is, 3 redundant SDs for each. The positive effect of this optimization is shown in the lower half of the table, where the failure rate is seen to reduce to a value of $639.46 \times 10^{-10}\ [FIT]$, representing a substantial improvement of over five orders of magnitude, which corresponds to a reliability value of 100% within the given stated mission time.

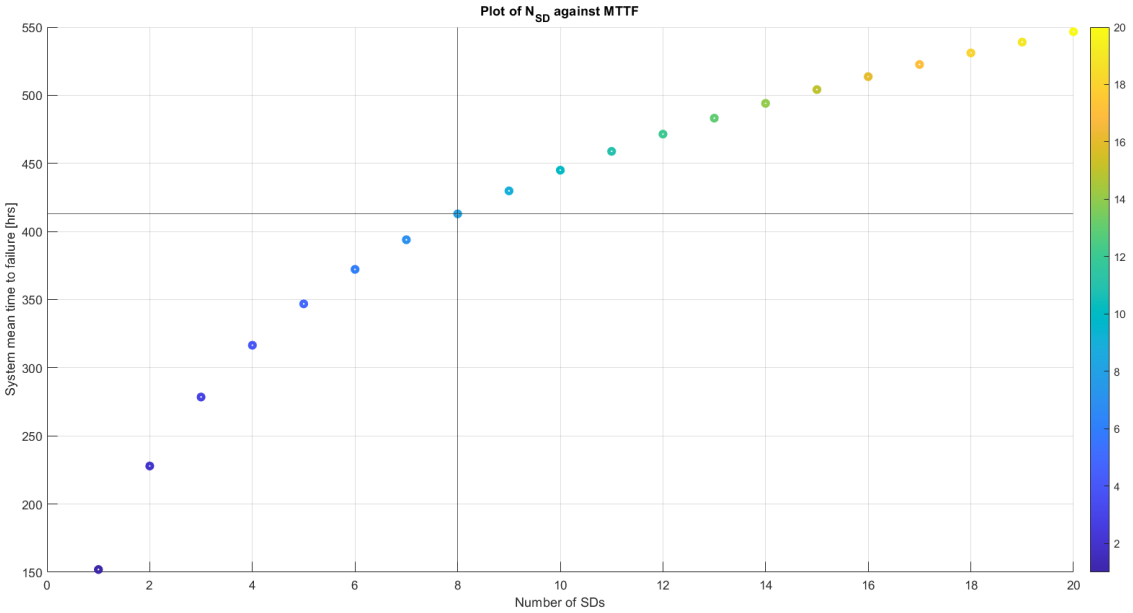


Figure 4.1: Plot of N_{SD} against MTTF.

The MTTF for the corresponding reliability is estimated to be 412.9352 $[hrs]$, which is almost three times its optimum single SD value. The values chosen for the application voltage and load current are approximately the same without redundancy. The optimal heat sink base, on the other hand, changes from $30mm$ to $45mm$, whereas the bond wire diameter changes from $400\mu m$ to $500\mu m$. The reason for this could be attributed to the necessity of accounting for the increase in SD components.

Figure 4.1 plots the change in MTTF value as the number of redundant SDs increases. It also gives key insight into how much the MTTF is improved when FTC via redundancy is incorporated into the optimization. This indicates a key tradeoff as the number of components can be sufficiently increased but goes against the total size, available space, and cost of the design. For this reason, the optimization algorithm returns 8 as the optimum number of SDs, given the design constraints that were set for the minimization objective function.

Single-objective optimization of the Cap's useful failure rate

The optimization of the capacitor's FR as the fitness function, as given in (3.62), also yields interesting results. Firstly, the optimization convergence occurs after 55 generations with an average of 0.06475 and a penalty value of 90.219×10^{-4} $[FIT]$. In comparison to the $\lambda_{S,SD}$ the capacitor system failure rate is poor, and tries to compensate for that with an increase in number of capacitors

in the component spacing with the available space on the pcb.

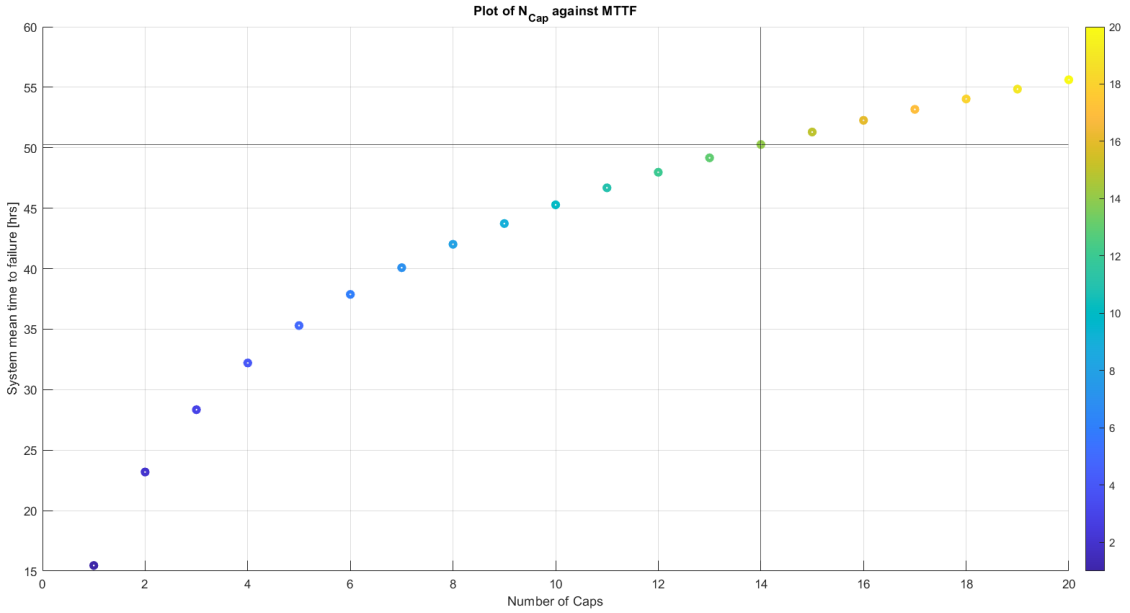


Figure 4.2: Plot of N_{Cap} against MTTF.

A critical observation of Table 4.6 also reveals further details about the capacitor FR SOOP. For one, the high FR of the $\lambda_{S,Cap}$ testifies to the fact that capacitors generally have a higher failure rate than switching device, hence the reason they are mostly discovered to be the faulty components during an inverter/converter system downtime. Another key point to note from the results is the different capacitor length and diameter that are selected based the option of redundancy.

Finally, an observation of the MTTF reveals the significance of redundancy as a means of reliability improvement. With 6 redundant capacitors for each main capacitor - given the above constraints - the capacitor system's MTTF rises from 15 hrs to 50 hrs, which is an appreciable improvement.

Single-objective optimization of the SD's cycles to failure

The cycles to failure maximization of the SD as formulated in the problem (3.64) yields its own optimization results as discussed in this section. Because this was a maximization problem, the mean penalty value came out negative with a manitude of 24897 cycles to failure.

Two key observations are made in Table 4.7. With the set of constraints identified in the first

Table 4.6: Capacitor failure rate optimization design results.

$\boldsymbol{\Delta}$	**Design parameter**	**Optimum Value**	**Constraint**	**Min/Max Value**
$1Cap$	$f_{sw}\,(kHz)$	37.085	$A_{Cap,max}\,[m^2]$	$\leq \frac{9\pi}{400}$
	$V_{applied}\,(V)$	519.35	AR_{Cap}	$1 \leq AR_{Cap} \leq 2$
	$L_{Cap}\,(mm)$	167.5	$I_{rip,max}\,[\%]$	≤ 50
	$D_{Cap}\,(mm)$	95	$Der\,[\%]$	≥ 80
	$\boldsymbol{\lambda_{0Cap}}\,[FIT]$		0.40	
	$\boldsymbol{\lambda_{Cap}}\,[FIT]$		646.85×10^{-4}	
	$\boldsymbol{R_S}(T)\,[\%]$		21.17	
	$\boldsymbol{MTTF}\,[hrs]$		15.4595	
$\geq 2\,Caps$	$f_{sw}\,(kHz)$	39.025	$A_{Cap,max}\,[m^2]$	$\leq \frac{9\pi}{400}$
	$V_{applied}\,(V)$	519.35	AR_{Cap}	$1 \leq AR_{Cap} \leq 2$
	$L_{Cap}\,(mm)$	157.5	$I_{rip,max}\,[\%]$	≤ 50
	$D_{Cap}\,(mm)$	85	$Der\,[\%]$	≥ 80
	N_{Cap}	14	$Space_{pcb}\,[\#]$	≤ 20
	$-$	$-$	$Budget_{Cap}\,[\$]$	≤ 750
	$\boldsymbol{\lambda_{S,Cap}}\,[FIT]$		90.219×10^{-4}	
	$\boldsymbol{R_S}(T)\,[\%]$		96.42	
	$\boldsymbol{MTTF}\,[hrs]$		50.2677	

optimization, the cycles to failure observed was 24.897×10^3, which is lower than the base cycles to failure of 28×10^3. In comparison to this, a change in the deration constraint from 80% to 65% yields a higher cycles to failure of 33.711×10^3, albeit at slightly different optimum parameters - a change from $25\,mm$ to $30\,mm$ in the heat sink base thickness.

A third observation is made when the heat sink size constraint is altered. Here, it is seen the cycles to failure did not change as much as was the case when the deration constraint what changed. Reliability improvement of the switching device's wear-out failure via deration seems to be the best choice for that case.

Table 4.7: Switching device cycles to failure optimization design results.

$\boldsymbol{\Delta}$	**Design parameter**	**Optimum Value**	**Constraint**	**Min/Max Value**
–	$f_{sw}\,(kHz)$	5.000	$T_{J,max}\,[^{\circ}C]$	≤ 125
	$i_{SD,c}\,(A)$	15.98	$Der\,[\%]$	≥ 80
	$V_{applied}\,(V)$	519.35	$A_{hs,max}\,[mm^2]$	$\leq 5000 \times 10^{-6}$
	$t_{hs,b}\,(mm)$	25	$i_{SD,c,max}\,[A]$	≤ 20
	$D_{SD,bw}\,(\mu m)$	300	–	–
	$\boldsymbol{N_{f0,SD}}$		28×10^3	
	$\boldsymbol{N_{f,SD}}$		24.897×10^3	
Der	$f_{sw}\,(kHz)$	5.000	$T_{J,max}\,[^{\circ}C]$	≤ 125
	$i_{SD,c}\,(A)$	12.98	$Der\,[\%]$	≥ 65
	$V_{applied}\,(V)$	500	$A_{hs,max}\,[mm^2]$	$\leq 5000 \times 10^{-6}$
	$t_{hs,b}\,(mm)$	30	$i_{SD,c,max}\,[A]$	≤ 20
	$D_{SD,bw}\,(\mu m)$	300	–	–
	$\boldsymbol{N_{f0,SD}}$		28×10^3	
	$\boldsymbol{N_{f,SD}}$		33.711×10^3	
A_{hs}	$f_{sw}\,(kHz)$	5.001	$T_{J,max}\,[^{\circ}C]$	≤ 125
	$i_{SD,c}\,(A)$	15.98	$Der\,[\%]$	≥ 80
	$V_{applied}\,(V)$	519.37	$A_{hs,max}\,[mm^2]$	$\leq 5000 \times 10^{-2}$
	$t_{hs,b}\,(mm)$	35	$i_{SD,c,max}\,[A]$	≤ 20
	$D_{SD,bw}\,(\mu m)$	300	–	–
	$\boldsymbol{N_{f0,SD}}$		28×10^3	
	$\boldsymbol{N_{f,SD}}$		24.896×10^3	

Single-objective optimization of the Cap's lifetime

Considering the initial constraints, the mean penalty value after convergence was 8.713, which corresponded to an optimum lifetime value of 9 years.

Table 4.8: Capacitor lifetime optimization design results.

$\boldsymbol{\Delta}$	**Design parameter**	**Optimum Value**	**Constraint**	**Min/Max Value**
–	$f_{sw}\,(kHz)$	7.985	$A_{Cap,max}\,[m^2]$	$\leq \frac{9\pi}{400}$
	$V_{applied}\,(V)$	519.35	AR_{Cap}	$1 \leq AR_{Cap} \leq 2$
	$L_{Cap}\,(mm)$	7.5	$I_{rip,max}\,[\%]$	≤ 50
	$D_{Cap}\,(mm)$	5	$Der\,[\%]$	≥ 80
	$\boldsymbol{L_0}\,[yrs]$		1	
	$\boldsymbol{L_{x,Cap}}\,[yrs]$		9.0039	
Der	$f_{sw}\,(kHz)$	7.985	$A_{Cap,max}\,[m^2]$	$\leq \frac{9\pi}{400}$
	$V_{applied}\,(V)$	500	AR_{Cap}	$1 \leq AR_{Cap} \leq 2$
	$L_{Cap}\,(mm)$	7.5	$I_{rip,max}\,[\%]$	≤ 50
	$D_{Cap}\,(mm)$	5	$Der\,[\%]$	≥ 65
	$\boldsymbol{L_0}\,[yrs]$		1	
	$\boldsymbol{L_{x,Cap}}\,[yrs]$		10.8862	
I_{rip}	$f_{sw}\,(kHz)$	6.885	$A_{Cap,max}\,[m^2]$	$\leq \frac{9\pi}{400}$
	$V_{applied}\,(V)$	519.35	AR_{Cap}	$1 \leq AR_{Cap} \leq 2$
	$L_{Cap}\,(mm)$	7.5	$I_{rip,max}\,[\%]$	≤ 58
	$D_{Cap}\,(mm)$	5	$Der\,[\%]$	≥ 80
	$\boldsymbol{L_0}\,[yrs]$		1	
	$\boldsymbol{L_{x,Cap}}\,[yrs]$		20.19	

The optimum frequency, application voltage, length, and diameter[2] of the capacitor were also determined for different constraint variations. The first notable difference is that whereas reducing the deration factor increased the lifetime by 1 year, the control parameters remained approximately the same, with the exception of the application voltage since increasing the deration meant reducing the percentage. Furthermore, an observation of Table 4.8 indicates regardless of the changes in deration or ripple current constraints, the minimum capacitor length and diameter are chosen as the optimum values. A similar result was obtained for a change in the overall surface area of the Cap,

[2]This research assumes a cylindrical-shaped capacitor.

albeit not shown here - the parameters remained approximately the same as the initial constraint conditions.

The major improvement can be seen in the lower part of Table 4.8 where the lifetime goes as high as 20 $years$ when the constraint of the ripple current is increased from 50% to 50%. In other words, if the application can tolerate a ripple current of 58% in reference to the load current, then that seems to be the best choice.

Multi-objective optimization of the SD's and Cap's useful failure rates

The Pareto frontier shown in Figure 4.3 is the set of non-dominated solutions where improvement in one objective (SD FR) can only be achieved by sacrificing the other (Cap FR). By reducing the failure rate of one component, the other might experience a corresponding increase. This is indicative of design choices that improve switching device reliability (e.g., using larger devices and derating currents or voltage) might come at the expense of capacitor stress (e.g., higher voltage ratings and larger physical sizes).

When the number of parallel components is included as a control parameter, as was the case for the SOOP, better optimization results are obtained. Although the failure rates of the capacitor did not change as much, those of the switching device were improved by a factor of 10. This can better be visualized in the parallel plot discussion below.

The parallel plot visualization in Figure 4.5 further offers valuable insights into the trade-off between switching device and capacitor failure rates in the optimization results. By visualizing each solution as a line across the two axes (one for each failure rate), potential trends and patterns can be identified, as was the case in the Pareto front. For instance, an observation of the parallel plot can reveal the specific design configurations that lead to lower failure rates for both components simultaneously are likely to be found in the median section of the solution data. These visual explorations complement the analysis of the Pareto frontier by providing a more intuitive understanding of how different design choices influence the failure rates of both critical components of the half-bridge power electronic converter (PEC). Another key observation worth noting is the differences in the SD and Cap failure rates as well as the MTTFs achieved at the extreme ends of the Pareto front as a result of including parallel redundancy in the GA optimization. This is tabulated in Table 4.9.

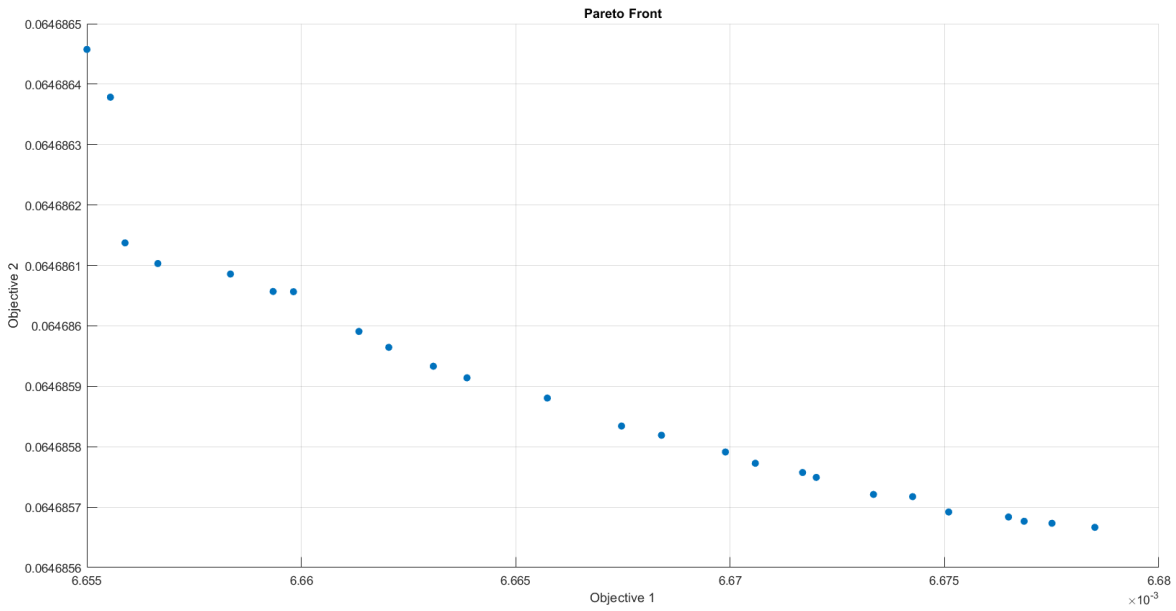


Figure 4.3: Pareto front of the Cap's and SD's failure rates.

As can be observed from the data presented in Table 4.9, a fascinating trend emerges regarding the selection of parallel components for fault tolerance in the PEC design. As can be observed from the data presented in Table 4.9, a fascinating trend emerges regarding the selection of parallel components for fault tolerance in the PEC design. We observe that when the FR of both switching devices is at its highest value, the GA appears to compensate by incorporating an increased number of parallel SD components. This strategy leverages redundancy to improve the overall system reliability. In essence, by having multiple SDs operating in parallel, the converter can potentially maintain functionality even if one device fails.

Table 4.9: multi-objective optimization of SD and Cap with parallel redundancy comparison.

	SD	**Cap**
$\boldsymbol{\lambda_{S,max}}$	1.05×10^{-04}	5.75×10^{-2}
$\boldsymbol{MTTF_{S,min}}$	3.33×10^{4}	6.08×10^{1}
$\boldsymbol{N_{Comp}}$	18	18
$\boldsymbol{\lambda_{S,min}}$	8.37×10^{-16}	4.38×10^{-3}
$\boldsymbol{MTTF_{S,max}}$	1.79×10^{15}	4.76×10^{2}
$\boldsymbol{N_{Comp}}$	2	4

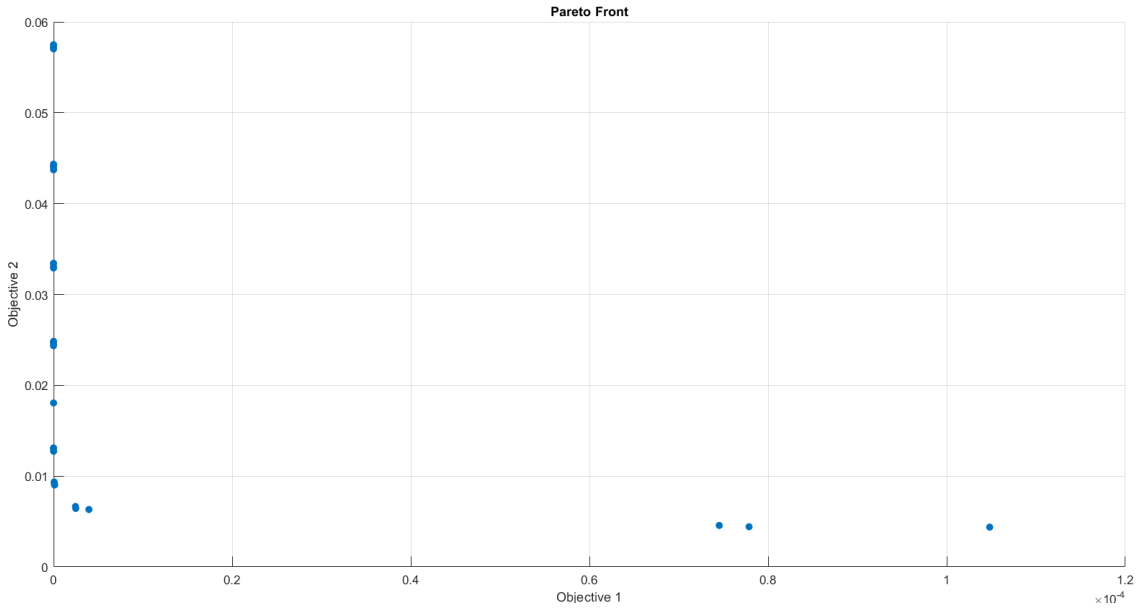
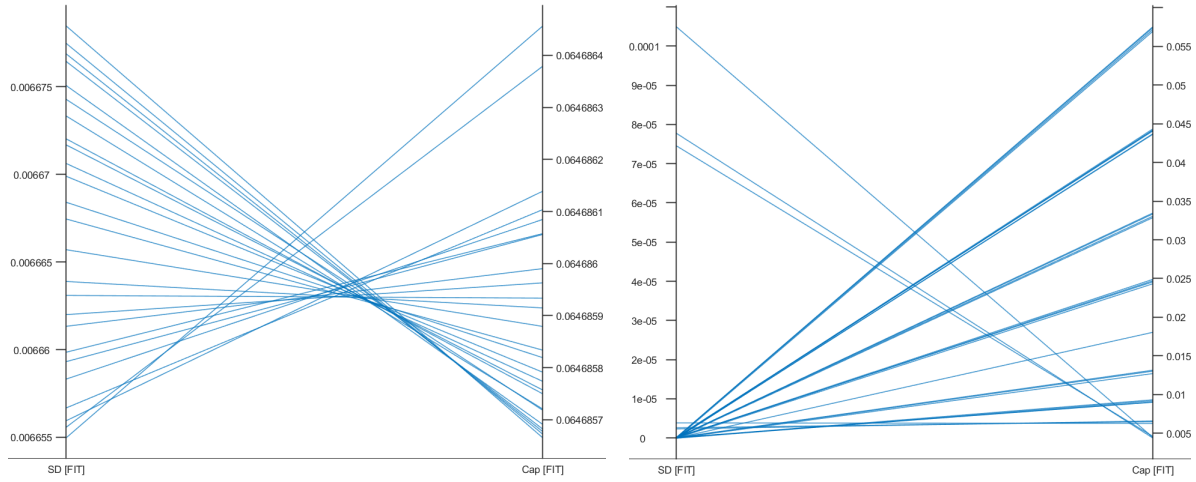


Figure 4.4: Pareto front of the Cap's and SD's failure rates taking parallel redundancy into account.



(a) (b)

Figure 4.5: (a) Parellel plot of the FR solution of the multi-objective optimization, (b) Parellel plot of the FR solution of the multi-objective optimization taking parallel redundancy into account.

Conversely, the situation presents a contrasting scenario when the FR of the Cap is at its maximum while the FR of the SDs remains at a minimum. In this case, the GA appears to prioritize the Cap by selecting the highest amount of components for parallel redundancy. This prioritization suggests that the potential consequences of a Cap failure might be deemed more detrimental to the system's functionality or safety compared to an SD failure, even though the SDs exhibit a higher

base FR in this specific instance.

By carefully analyzing the interplay between component FRs and the selection of parallel components, as revealed in Table 4.9, we gain valuable insights into the decision-making process employed by the optimization algorithm. This understanding can be crucial for further refining the optimization process or for making informed design choices when balancing component selection, redundancy strategies, and overall system reliability.

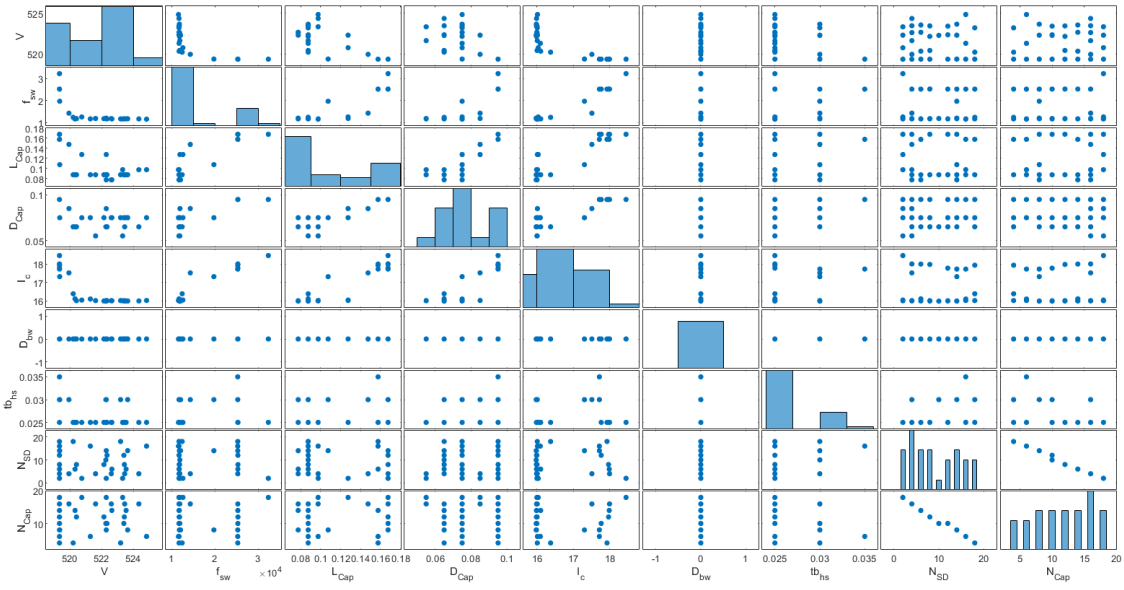


Figure 4.6: Scatter plot of the optimal control parameters for the FR multi-objective optimization, taking parallel redundancy into account.

The optimum parameter solutions on the other hand is best visulized via the scatter plot in Figure 4.6. Some key insights show that whereas the optimum application voltage ($V_{applied}$) is clustered around the minimum derated value, the optimum switching frequencies (f_{sw}) vary between $9\,kHz$ and $12\,kHz$. Similarly, lower optimum collector current ($i_{SD,c}$) correspond to lower optimum bond wire diameters ($D_{SD,bw}$). The observation made with the number of component selection interplay is also shown by the parallel plot.

Multi-objective optimization of the SD's and Cap's wear-out failure rates

The optimization undertaken in this section aimed to achieve an equilibrium between the cycles to failure of the switching device (SD), and the lifetime of the capacitor (Cap). Three

results, visually presented in a Pareto frontier plot, unveil the intriguing interplay – the trade-off – between these two vital components' ability to withstand operational stresses over extended periods. Solutions positioned closer to the vertical axis of the plot represent the lifetime of the Cap while simultaneously achieving remarkably long SD cycles to failure. Conversely, solutions gravitating towards the lower right corner prioritize the SD's cycles to failure but at the expense of the Cap's lifetime.

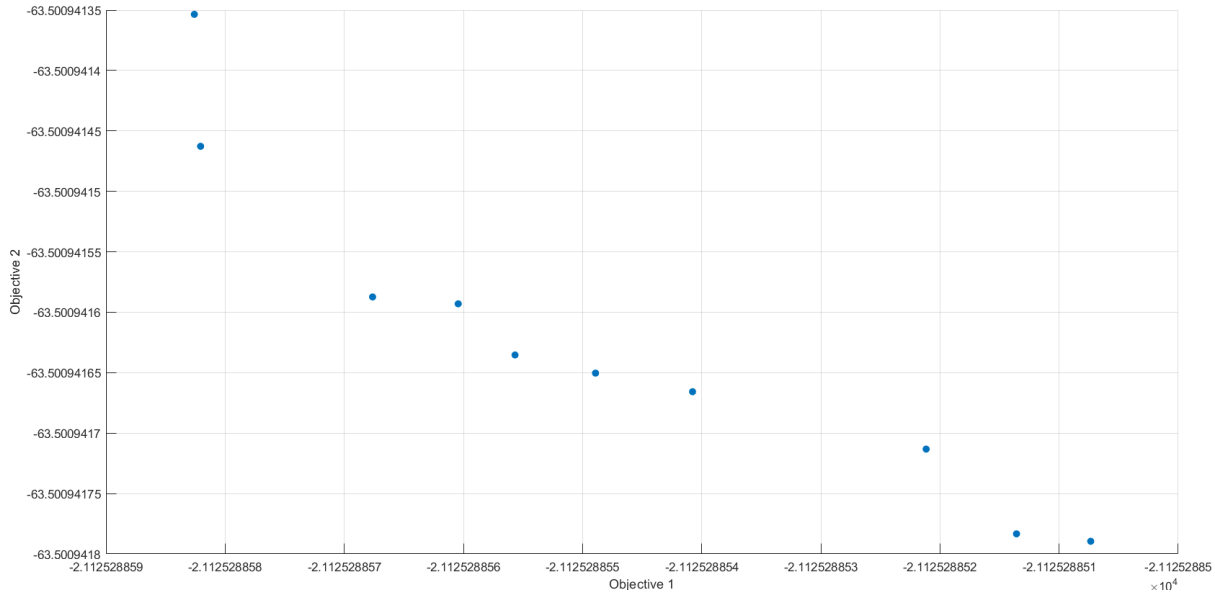


Figure 4.7: Pareto front of the Cap's lifetime and SD's cycles to failure at an increased percent ripple current constraint.

Since maximizing the overall lifespan of the PEC is the ultimate objective, a solution strategically situated closer to the middle of the Pareto frontier might be the most compelling choice. This design configuration prioritizes both the SD's ability to endure a high number of switching cycles and the Cap's ability to function reliably over a prolonged period. However, if the application necessitates frequent switching cycles for the SD, perhaps to accommodate a high-speed control scheme, a solution positioned towards the lower right corner could be more suitable. This design might prioritize maximizing SD cycles to failure, even if it comes at the expense of a slightly reduced capacitor lifetime.

By increasing the ripple current constraint on the multi-objective optimization, a different pareto front showing how much the capacitor's lifetime can be improved is plotted. The switching device's cycles to failure on the other hand is best influenced by the deration when the deration constraint

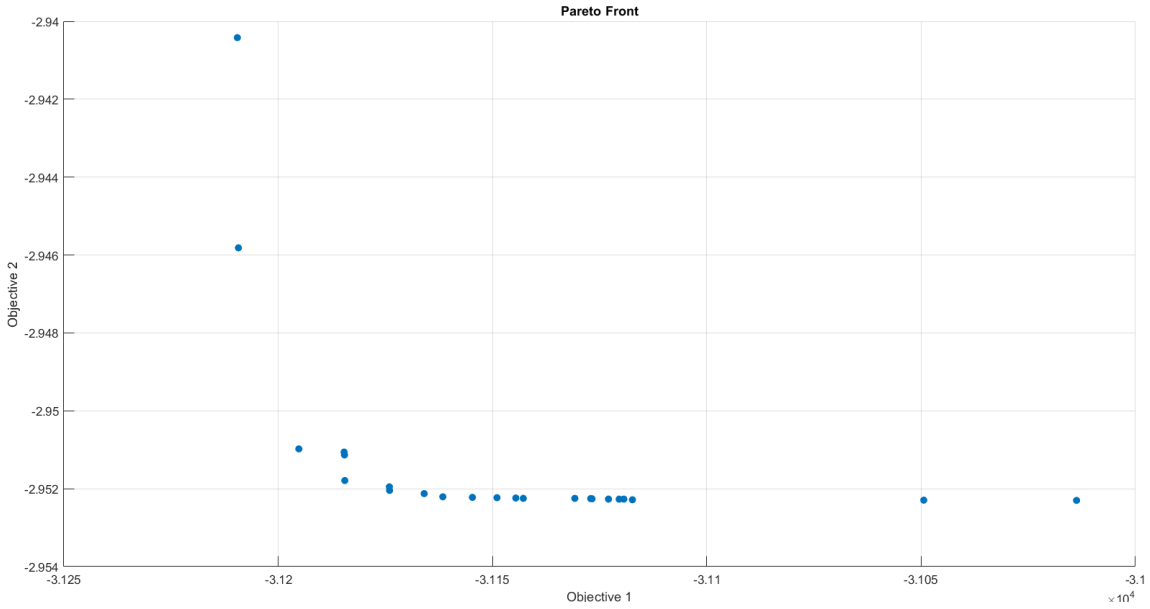
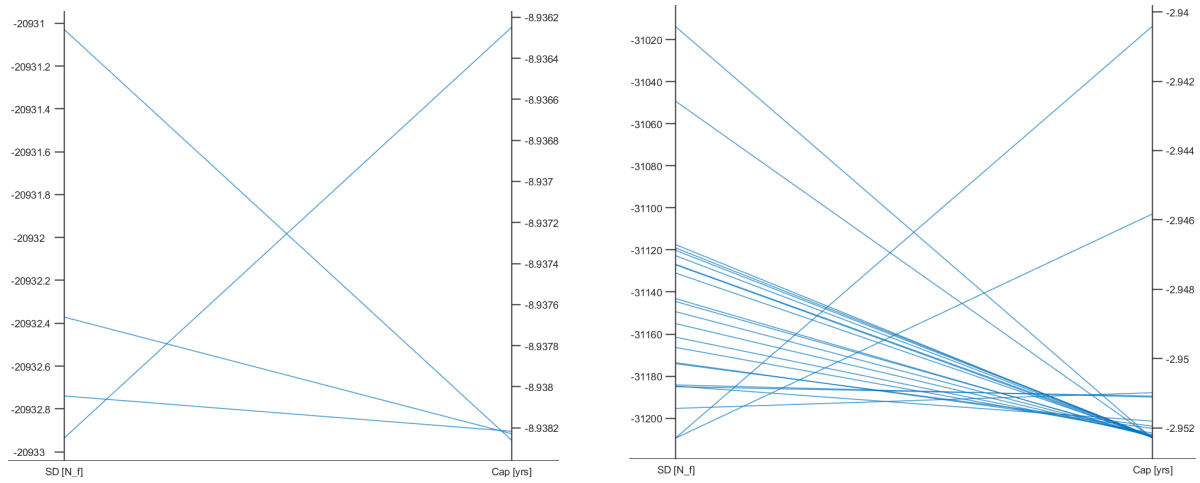


Figure 4.8: Pareto front of the Cap's lifetime and SD's cycles to failure at a decreased deration constraint.

is decreased from 80% to 65%. However, this is achieved at the expense of the capacitor's lifetime.

Figure 4.9 serves as a valuable visual tool, where each plot unveils a distinct perspective on the optimization process. Here, subplot (a) portrays the parallel plot results obtained using the initial set of constraint conditions, while subplot (b) depicts the consequences of varying the voltage deration constraint for the SD. A meticulous examination of both parallel plots in conjunction with the corresponding Pareto frontiers above, allows us to pinpoint the constraints that exert the most significant influence on the reliability of the components. Through this analysis, two key constraints emerge as the primary drivers of both lifetime and cycles to failure: the voltage deration factor for the SD and the ripple current limitation for the Cap.

Examining subplot (a) of Figure 4.9, we can observe how the initial constraint conditions influence the distribution of solutions within the plot. By tracing the lines representing individual solutions across the various axes (one for each parameter), we can potentially identify trends and relationships between the chosen constraints and the resulting SD cycles to failure and capacitor lifetime. For instance, a clustering of solutions towards a particular region of the plot might suggest a correlation between specific constraint values and favorable outcomes in terms of component reliability.



(a) (b)

Figure 4.9: (a) Parellel plot of the lifetime and cycles to failure solutions of the multi-objective optimization at initial constraints, (b) Parellel plot of the lifetime and cycles to failure solution of the multi-objective optimization at a decreased deration value.

Subplot (b) in Figure 4.9 presents a fascinating contrast. Here, the deration constraint for the SD is no longer fixed, but rather allowed to vary within a specified value of 60%. By comparing this plot with subplot (a), we can directly observe the impact of this variable constraint on the Pareto frontier and the overall distribution of solutions. This comparison might reveal a shift in the frontier, potentially indicating an improvement in either SD cycles to failure or capacitor lifetime (or potentially both) due to the flexibility offered by the voltage deration.

The above analysis is further expanded on by an examination of the scatter plots of the optimal solutions. Considering Figure 4.10, the optimal switching frequencies increase toward an average of 7.985 kHz whearas the capacitor length and diameter seem to increase albeit with minute voltage increment. The optimal SD collector current has an approximately inverse exponential relationship with both the voltage and the switching frequency.

In other words, the scatter plots for the optimal solutions offer some more technical insights into the design choices made by the GA optimization algorithm. By analyzing these plots, we can potentially identify trends and relationships between various design parameters that contribute to achieving the optimal balance between the SD cycles to failure and capacitor lifetime.

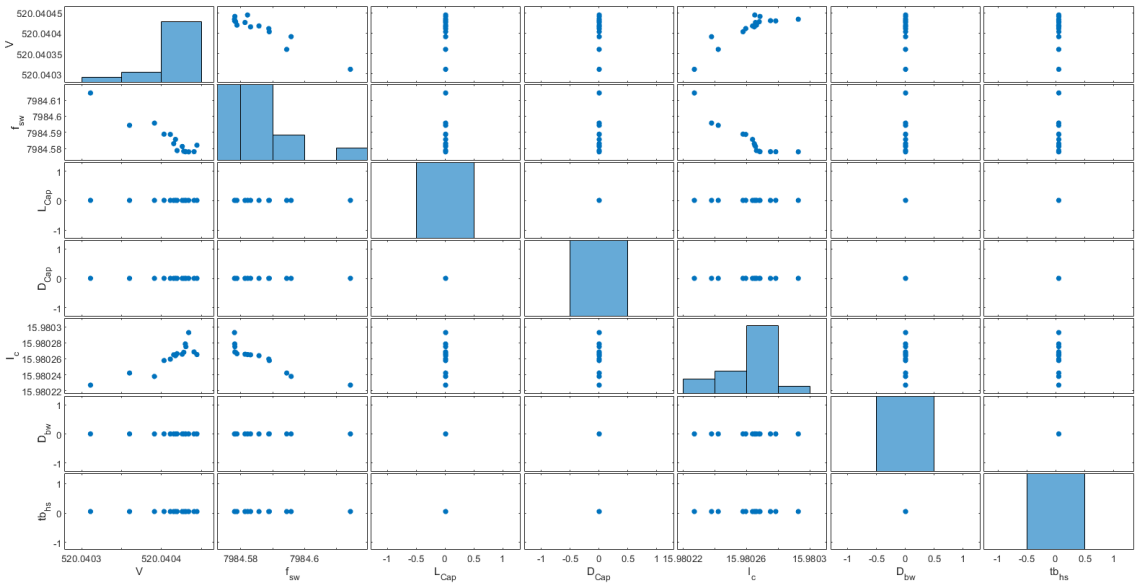


Figure 4.10: Scatter plot of the optimal parameters for the wear-out multi-objective optimization at a decreased deration constraint.

As mentioned above, one intriguing plot to explore is the one depicting the relationship between voltage and switching frequency. In this case, designs with higher operating voltages tend to favor lower switching frequencies. This could be due to the trade-off between voltage stress and switching losses on the SD. Higher voltages can stress the device, potentially leading to earlier failures. Conversely, reducing the switching frequency lowers switching losses but might necessitate the use of larger output capacitors.

Another scatter plot worthy of examination is the one relating collector current to bond wire diameter. Here, we might expect a positive correlation. Designs with higher collector currents flowing through the SD necessitate thicker bond wires to handle the increased current density and thermal load effectively. Insufficient bond wire diameter could lead to overheating and premature bond wire failures.

The scatter plot for heat sink base thickness can reveal insights into the thermal management strategies employed by the optimization algorithm. Thicker heat sinks generally offer better heat dissipation capabilities, which is crucial for maintaining the SD within its safe operating temperature range. However, thicker heat sinks also add weight and volume to the converter. The plot might show a trend where designs with higher switching frequencies or collector currents favor thicker heat

sinks to manage the increased thermal load.

CHAPTER 5

SUMMARY

Power electronic converters (PECs) are ubiquitous in modern technology, driving advancements in renewable energy systems, electric vehicles (EVs), and various industrial applications. However, their reliability is often hindered by the finite lifetimes of switching devices (SDs) and capacitors (Caps) - the two failure-critical components in a converter. This thesis investigated methods to optimize PEC design for a balanced trade-off between these critical components' longevities, ultimately enhancing overall converter reliability.

This thesis employed Genetic Algorithm (GA), a powerful evolutionary optimization technique, to explore the design space of PECs. The GA considered various design parameters, including:

- Voltage
- Switching frequency
- Collector current
- Bond wire diameter
- Heat sink characteristics (base thickness)
- Capacitor dimensions (length and diameter)
- Number of parallel components

The optimization process aimed to achieve four primary objectives:

1. Minimize the switching device failure rate
2. Minimize the capacitor failure rate
3. Maximize switching device cycles to failure
4. Maximize capacitor lifetime

Pareto frontier visualization technique, parallel plots, and scatter plots were used to represent the trade-off between these objectives, allowing for informed decision-making when selecting an optimal PEC design.

Key results of the work

The research revealed crucial insights into the constraints impacting component reliability. Deration for the switching device and ripple current limitation for the capacitor were identified as the most influential factors.

Scatter plots of optimal solutions provided valuable information regarding the optimization algorithm's design choices. These plots suggested trends between: Voltage and switching frequency, collector current and bond wire diameter, heat sink base thickness and thermal management strategies, capacitor dimensions and lifetime considerations.

This analysis provides a deeper understanding of the design space for PECs, enabling engineers to make more informed decisions when optimizing for reliability, performance, size, and cost constraints.

Contributions

This thesis advances the field of power electronics by establishing a framework for optimizing PEC design for a balanced trade-off between switching device failure rate and cycles to failure, and capacitor failure rate and lifetime. The insights gleaned from the single as well as the multi-objective optimization with GA and the analysis of design parameters empower engineers to develop more reliable and efficient PECs.

Limitations of the research

Although this research considers a holistic approach to selecting the best PoF models to represent the power electronic converter's reliability, it falls short in some aspects, including but not limited to the following:

- It is assumed that the free-wheeling body diode of the IGBT forms part of the SD's failure rate contribution. In reality this is not always the case. The losses due to the reverse recovery action of the body diode is therefore not taken into acount in the losses estimation.
- A few maximum values (worst case) had to be assumed in cases where variables to be estimated depended on a post-determined variable. The effect of this approximation where then reflected in the results.
- The switching device is assumed to be a power IGBT and all estimations and simulations were based on this assumption. In that regard, the thesis is limited as the parameters and dynamics of a MOSFET or any other type of SD for that matter may vary from that of the IGBT.
- The switching energy loss (E_{sw}) equation does not seperate the dynamics of E_{on} and E_{off}, and assumes a bulk sum. This is done to reduce the mathematical complexity and also because of the lack of a sufficient model that properly represents both switching dynamics.
- The estimation of the heat sink area assumes a rectangular/cuboid shape and does not factor in modern heat sink design, including the fin-shape, etc.
- The capacitor type assumed for the problem formulation is the snap-in aluminum electrolytic type with a cylindrical shape, and other types and variants are not considered.
- The optimization design exploration space is limited to a few design parameters to minimize the computational complexity demanded by the algorithm.
- The problem formulation is centered on a sample available datasheet of some chosed component, and must not be applied as a general case for SDs and Caps.
- The problem formulation is based only on the two predominant components also called failure-prone components. In reality, other components, including but not limited to the PCB and sensors for health management, can also contribute to the converter's failure.

Suggestions for future work

While this research focused on heat sink sizing, junction temperature, bond wire current-capability, deration, ripple current, spacing, and cost constraint, expanding the optimization frame-

work to encompass additional constraints or objectives, such as converter efficiency or cost or even power density could yield more insights.

Analysis and incorporation of the PEC's control, that is the health and prognostics method of reliaibility improvement into the optimization to account for that will also prove advantageous.

Experimental validation of the optimization results using real-world converter prototypes to verify the practical effectiveness of the proposed methods is also another consideration.

Finally, it could be worth exploring alternative optimization algorithms and comparing their performance with the GA for PEC design optimization.

Conclusions

This work presented both single and multi-objective optimization approach using Genetic Algorithm (GA) to enhance the reliability of power electronic converters (PECs). The optimization focused on achieving a desirable balance between optimizing the two reliability phases of the two failure-prone components in a power electronic converter (PEC), that is, switching devices (SDs) and capacitors (Caps). The key contribution of this work lies in establishing an optimization problem formulation that leverages the strengths of GA for PEC reliability improvement. By simultaneously considering four critical longevity aspects (failure rate and cycles to failure for the SD and failure rate and lifetime for the capacitor), the framework facilitates the design of PECs with improved overall reliability. The analysis of optimal solutions revealed significant insights into the chosen design space. The observed trends between the application voltage, switching frequency, collector current, bond wire diameter, heat sink characteristics, and capacitor dimensions provide valuable guidance and insights when making informed design decisions that prioritize reliability improvement.

While this work demonstrates the effectiveness of the proposed framework, further exploration is warranted in several areas including but not limited to constraint refinement, where future research could focus on refining the key constraints identified in this research (deration for SD and ripple current for capacitor) by incorporating additional factors specific to different PEC applications. This could lead to even more targeted and effective optimization. Secondly, hybrid optimization techniques, where exploring the potential benefits of combining the GA with other optimization

algorithms, could potentially enhance the search process and lead to the discovery of even better design solutions for PECs. Thirdly, multi-criteria decision-making could be considered, which could provide a more holistic approach to selecting the optimal PEC design solution. This would allow for the incorporation of additional factors beyond just the four mentioned objective functions, such as cost, size, and thermal management considerations.

By continuing research along these lines, we can further refine the optimization design space and constraints, leading to the development of highly reliable and efficient PECs that meet the specific needs of diverse applications. Ultimately, this work paves the way for advancements in power electronics design, contributing to the development of more robust and reliable electrical systems.

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